IGLOO2 FPGAs

Introduction

Microsemi's IGLOO®2 FPGAs integrate fourth generation flash-based FPGA fabric and high performance communications interfaces on a single chip. The IGLOO2 family is the industry's lowest power, most reliable, and the most secure programmable logic solution. This next generation IGLOO2 architecture offers up to 3.6X gate count implemented with 4-input look-up table (LUT) fabric with carry chains, giving 2X performance, and includes multiple embedded memory options and math blocks for digital signal processing (DSP).

High speed serial interfaces include PCI EXPRESS® (PCIe®), 10 Gbps attachment unit interface (XAUI)/XGMII extended sublayer (XGXS) plus native serialization/deserialization (SERDES) communication, while double data rate 2 (DDR2)/DDR3 memory controllers provide high speed memory interfaces.

IGLOO2 Device Status

Family Devices	Status
M2GL005	Advance
M2GL010T/M2GL010	Advance
M2GL025T/M2GL025	Advance
M2GL050T	
M2GL050	Advance
M2GL090T/M2GL090	Advance
M2GL100T/M2GL100	Advance
M2GL150T/M2GL150	Advance

IGLOO2 Product Brief and Pin Descriptions

The product brief and pin descriptions are published separately:

IGLOO2 Product Brief

IGLOO2 Pin Descriptions

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Microsemi

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General Specifications

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Stresses beyond those listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 2-2 on page 2-2 is not implied.

Table 1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits		Units	Notes
		Min.	Max.		
VDD	DC core supply voltage. Must always power this pin.	–0.3	1.32	V	
VDD_2V5	DC Bias supply voltage. Must always power this pin.	–0.3	2.75	V	
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	–0.3	3.63	V	
MDDR_PLL_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	–0.3	3.63	V	
PLL0_PLL1_MDDR_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0–5	–0.3	3.63	V	
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	–0.3	3.63	V	
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply.	–0.3	2.75	V	
SERDES_[01]_L[0123]_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.	–0.3	1.32	V	
SERDES_[01]_VDD	PCIe/PCS power supply	–0.5	1.32	V	
VDDIx	DC FPGA I/O buffer supply voltage for MSIO I/O bank	–0.3	3.63	V	
	DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	–0.3	2.75	V	
VI	I/O Input voltage for MSIO I/O bank	–0.3	3.63	V	
	I/O Input voltage for MSIOD/DDRIO I/O bank	–0.3	2.75	V	
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	–0.3	3.63	V	
T_{STG}	Storage temperature	–65	150	°C	1
T_J	Junction temperature	–	125	°C	

Note:

1. *For flash programming and retention maximum limits, refer to Table 3 on page 11. For recommended operating conditions, refer to Table 2 on page 10.*

Table 2 • Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
T_J	Operating junction temperature	Commercial	0	25	85	°C	
		Industrial	–40	25	100	°C	
	Programming junction temperatures	Commercial	0	25	85	°C	
		Industrial	0	25	85	°C	
VDD	DC core supply voltage. Must always power this pin.		1.14	1.2	1.26	V	
VDD_2V5	DC Bias supply voltage. Must always power this pin.	1.2 V range	1.14	1.2	1.26	V	
		2.5 V range	2.375	2.5	2.625	V	
VPP	Power supply for charge pumps (for normal operation and programming)	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL0_PLL1_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0 to PLL5	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL Lane0 to Lane3. This is a +2.5 V SERDES internal PLL supply.		2.375	2.5	2.625	V	
SERDES_[01]_L[0123]_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.		1.14	1.2	1.26	V	
SERDES_[01]_VDD	PCIe/PCS power supply		1.14	1.2	1.26	V	
VDDIx	1.2 V DC supply voltage		1.14	1.2	1.26	V	
	1.5 V DC supply voltage		1.425	1.5	1.575	V	
	1.8 V DC supply voltage		1.71	1.8	1.89	V	
	2.5 V DC supply voltage		2.375	2.5	2.625	V	
	3.3 V DC supply voltage		3.15	3.3	3.45	V	
	LVDS differential I/O		2.375	2.5	3.45	V	
	B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O		2.375	2.5	2.625	V	
	LVPECL differential I/O		3.15	3.3	3.45	V	
VREFx	Reference voltage supply for FDDR (bank 0) and MDDR (bank 5)		0.49 * VDDIx	0.5 * VDDIx	0.51 * VDDIx	V	
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	

Table 3 • **FPGA and Embedded Flash Programming, Storage, and Operating Limits**

Product Grade	Storage Temperature	Programming Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. T_J = 0°C Max. T_J = 85°C	Min. T_J = 0°C Max. T_J = 85°C	FPGA	500	20 years
		Min. T_J = 0°C Max. T_J = 85°C	Embedded flash	< 1,000	20 years
				< 10,000	10 years
Industrial	Min. T_J = –40°C Max. T_J = 100°C	Min. T_J = 0°C Max. T_J = 85°C	FPGA	500	20 years
		Min. T_J = –40°C Max. T_J = 100°C	Embedded flash	< 1,000	20 years
				< 10,000	10 years

Thermal Characteristics

Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P} \qquad \textit{EQ 1}$$

$$\theta_{JB} = \frac{T_J - T_B}{P} \qquad \textit{EQ 2}$$

$$\theta_{JC} = \frac{T_J - T_C}{P} \qquad \textit{EQ 3}$$

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 4 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
M2GL005						
FG484	TBD	TBD	TBD	TBD	TBD	°C/W
VF400	TBD	TBD	TBD	TBD	TBD	°C/W
M2GL010						
FG484	18.2	14.8	13.6	8.8	4.9	°C/W
VF400	TBD	TBD	TBD	TBD	TBD	°C/W
M2GL025						
FG484	TBD	TBD	TBD	TBD	TBD	°C/W
VF400	TBD	TBD	TBD	TBD	TBD	°C/W
M2GL050						
FG484	15.3	12.2	11	6.3	3.2	°C/W
FG896	14.7	12.5	10.9	7.2	4.9	°C/W
VF400	TBD	TBD	TBD	TBD	TBD	°C/W
M2GL090						
FG676	TBD	TBD	TBD	TBD	TBD	°C/W
FG484	TBD	TBD	TBD	TBD	TBD	°C/W
M2GL100						
FC1152	TBD	TBD	TBD	TBD	TBD	°C/W
M2GL150						
FC1152	TBD	TBD	TBD	TBD	TBD	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where

θ_{JA} = 14.7°C/W (taken from Table 4 on page 12).

T_A = 85°C

$$\text{Maximum Power Allowed} = \frac{100°C - 85°C}{14.7°C/W} = 1.088\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculating Power Dissipation

Quiescent Supply Current

Table 5 • **Quiescent Supply Current Characteristics**

Power Supplies/Blocks	Modes and Power Supplies		Notes
	Non-Flash*Freeze mode	Flash*Freeze mode	
FPGA Core	On	Off	
VDD / SERDES_[01]_VDD	On	On	1
VPP / VPPNVM	On	On	
MDDR_PLL_VDDA / FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA / PLL0_PLL1_MDDR_VDDA	0 V	0 V	
SERDES_[01]_PLL_VDDA	0 V	0 V	3
SERDES_[01]_L[0123]_VDDAPLL / VDD_2V5	On	On	3
SERDES_[01]_L[0123]_VDDAIIO	On	On	3
VDDIx	On	On	2, 4
VREFx	On	On	
RAM	On	Sleep state	
HPMS Controller	50 MHz	50 MHz	
50 MHz Oscillator (enable/disable)	Enabled	Disabled	
1 MHz Oscillator (enable/disable)	Disabled	Disabled	
Crystal Oscillator (enable/disable)	Disabled	Disabled	

Notes:

1. *SERDES_[01]_VDD Power Supply is shorted to VDD.*
2. *VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI bank supplies. For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the IGLOO2 Board Design Guidelines application note.*
3. *SERDES and DDR blocks to be unused.*
4. *No Differencial (i.e. LVDS) I/O's or ODT attributes to be used.*

Table 6 • **Quiescent Supply Current**

Parameter	Modes	Conditions	M2GL050T VDD = 1.2 V	Units
IDC1	Non-Flash*Freeze mode	Typical conditions (25°C)	7.5	mA
IDC2	Flash*Freeze mode	Typical conditions (25°C)	0.387	mA

Average Fabric Temperature and Voltage Derating Factors

Table 7 • **Average Temperature and Voltage Derating Factors for Fabric Timing Delays (normalized to T_J = 85°C, worst-case VDD = 1.14 V)**

Array Voltage VDD (V)	Junction Temperature (°C)					
	–40°C	**0°C**	**25°C**	**70°C**	**85°C**	**100°C**
1.14	0.83	0.89	0.92	0.98	1.00	1.02
1.2	0.75	0.80	0.83	0.89	0.90	0.92
1.26	0.69	0.73	0.76	0.81	0.83	0.84

Timing Model

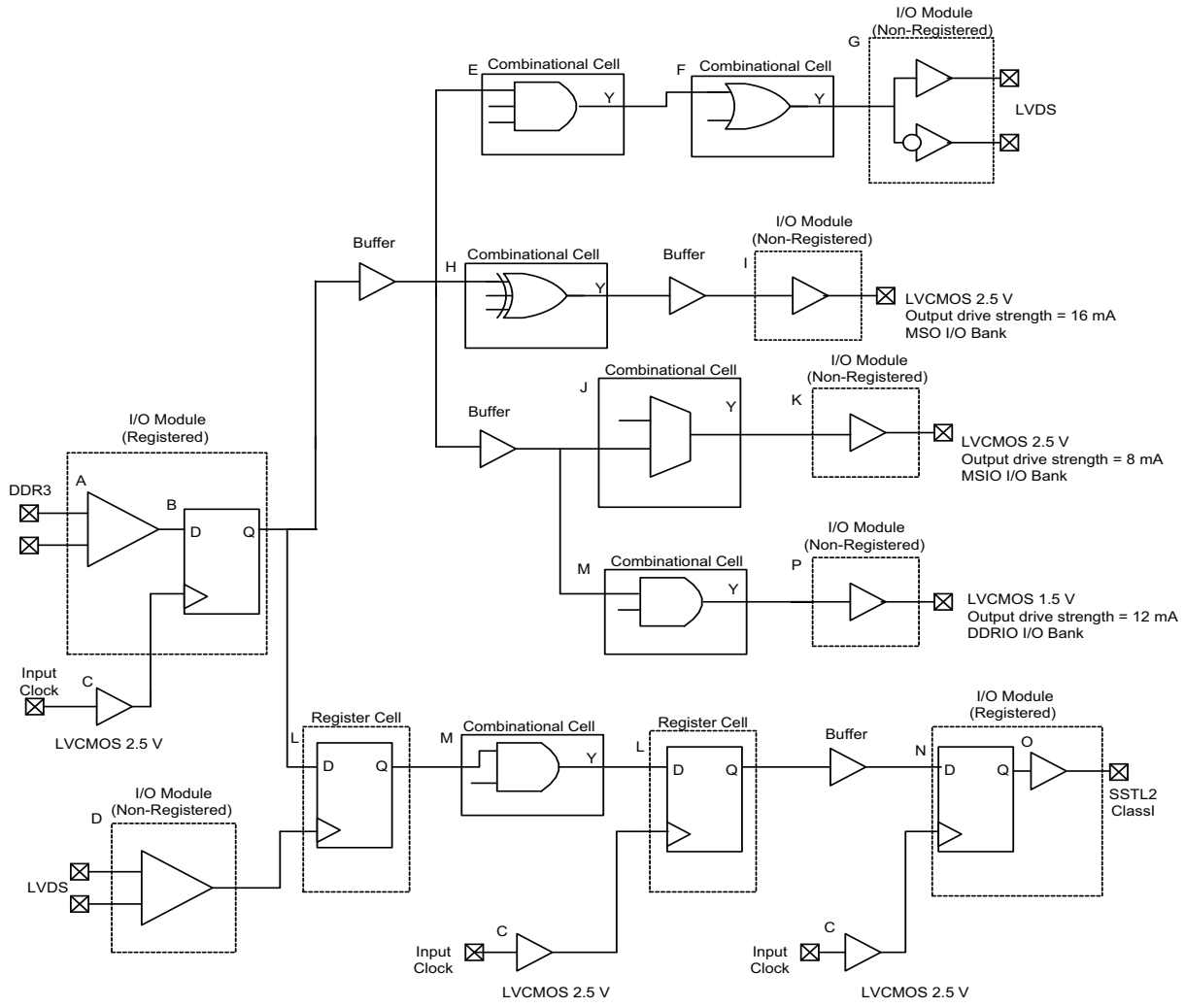


Figure 1 • **Timing Model**

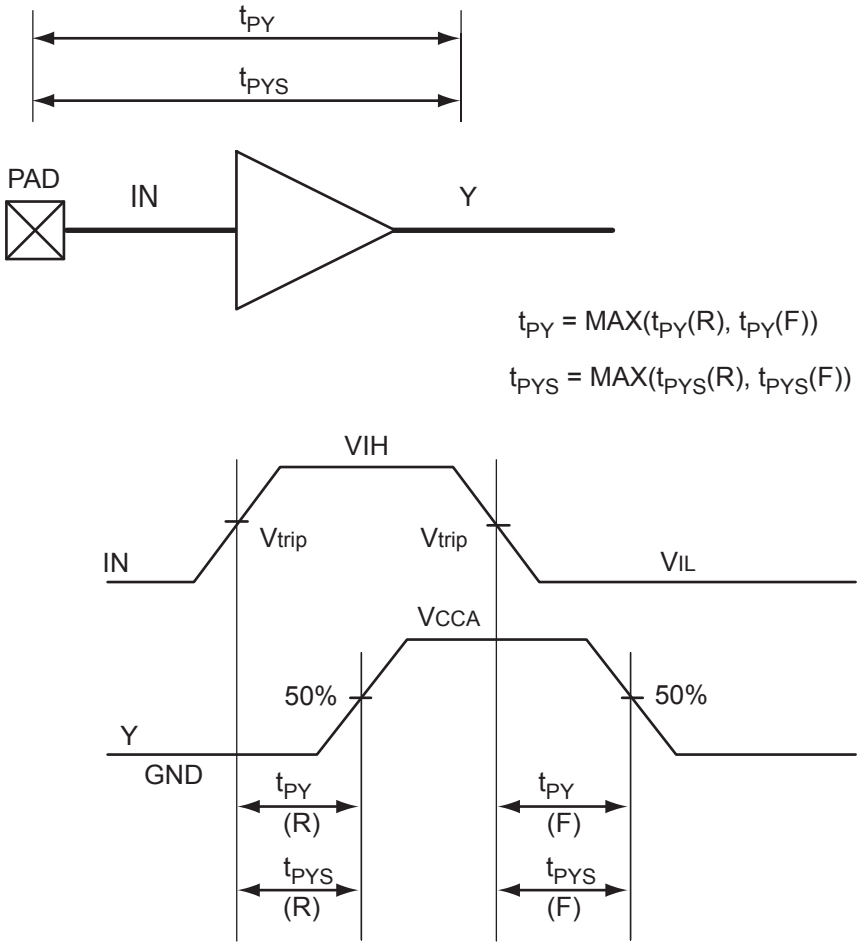
Table 8 • Timing Model Parameters

Index	Parameter	Description	-1	Units	For more information
A	t_{PY}	Propagation delay of DDR3 receiver (ODT=None)	1.662	ns	Refer to page 53
B	t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.168	ns	Refer to page 67
	t_{ISUD}	Setup Time of the Input Data Register	0.376	ns	Refer to page 67
C	t_{RCKH}	Input High Delay for Global Clock	1.611	ns	Refer to page 80
	t_{RCKL}	Input Low Delay for Global Clock	0.871	ns	Refer to page 80
D	t_{PY}	Input Propagation Delay of LVDS Receiver	2.835	ns	Refer to page 57
E	t_{DP}	Propagation Delay of a three input AND Gate	0.208	ns	Refer to page 77
F	t_{DP}	Propagation Delay of an OR Gate	0.172	ns	Refer to page 77
G	t_{DP}	Propagation Delay of a LVDS Transmitter	2.136	ns	Refer to page 57
H	t_{DP}	Propagation Delay of a three input XOR Gate	0.253	ns	Refer to page 77
I	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 16 mA on the MSIO Bank	2.412	ns	Refer to page 25
J	t_{DP}	Propagation Delay of a two input NAND Gate	0.172	ns	Refer to page 77
K	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 8 mA on the MSIO Bank	2.309	ns	Refer to page 25
L	t_{CLKQ}	Clock-to-Q of the Data Register	0.114	ns	Refer to page 79
	t_{SUD}	Setup Time of the Data Register	0.267	ns	Refer to page 79
M	t_{DP}	Propagation Delay of a two input AND Gate	0.172	ns	Refer to page 77
N	t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.277	ns	Refer to page 70
	t_{OSUD}	Setup Time of the Output Data Register	0.2	ns	Refer to page 70
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.055	ns	Refer to page 45
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12 mA, fast slew on the DDRIO Bank	3.316	ns	Refer to page 32

User I/O Characteristics

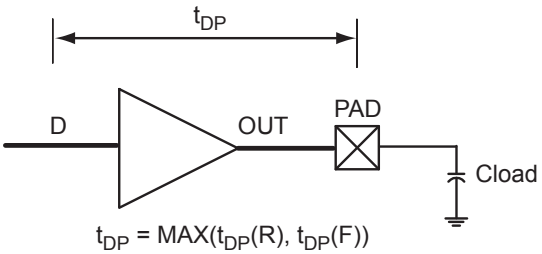
There are three types of I/Os supported in the IGLOO2 FPGA Family: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the "I/Os" section of the *IGLOO2 FPGA Fabric Architecture User's Guide*.

Input Buffer and AC Loading



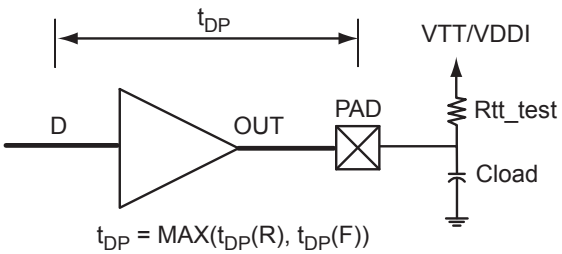
Output Buffer and AC Loading

Single-Ended I/O Test Setup



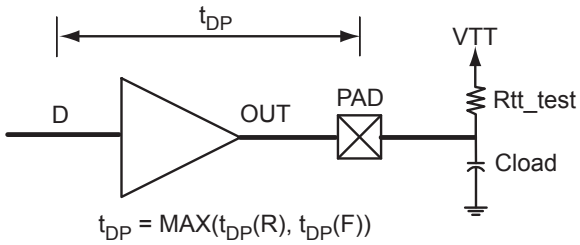
$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

HSTL/PCI Test Setup



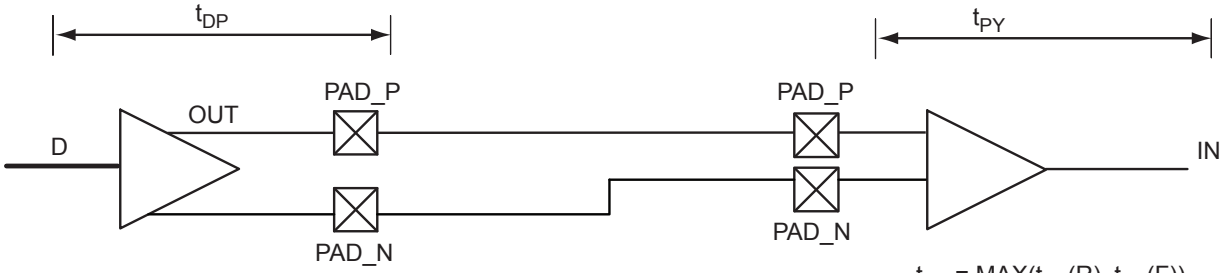
$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

Voltage-Referenced, Singled-Ended I/O Test Setup



$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

Differential I/O Test Setup



$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$

$t_{PYS} = MAX(t_{PYS}(R), t_{PYS}(F))$

Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 2.

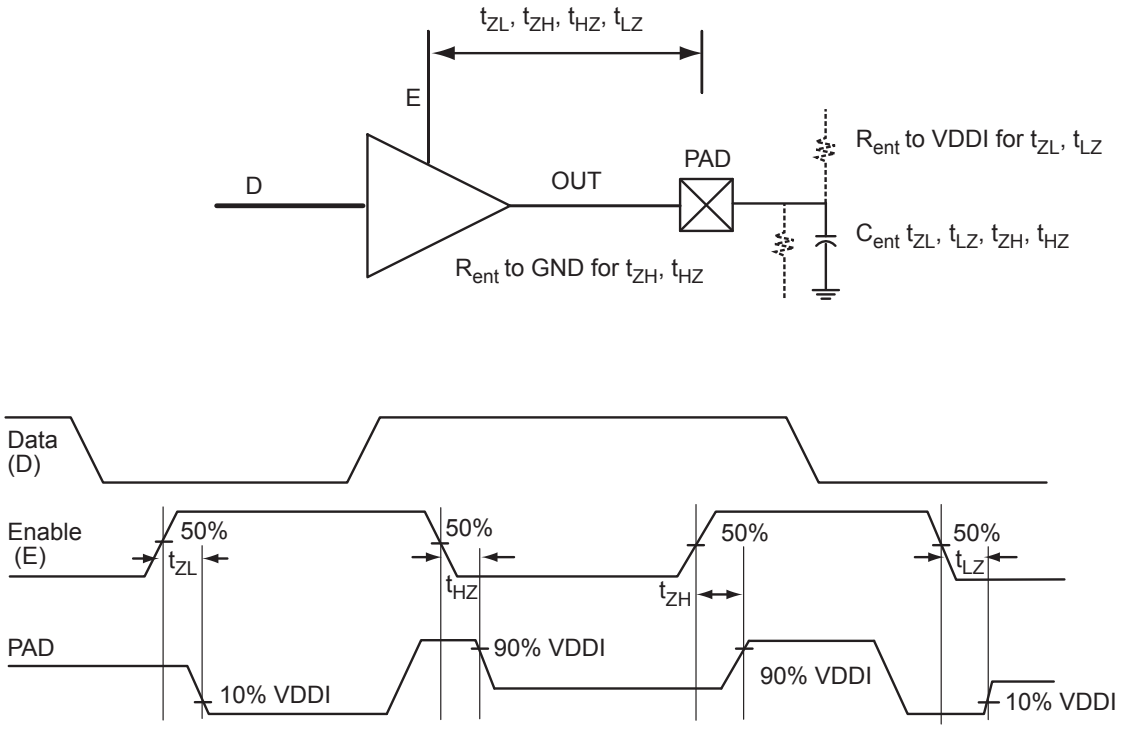


***Figure 2* • Tristate Buffer for Enable Path Test Point**

Detailed I/O Characteristics

Table 9 • Input Capacitance

Symbol	Definition	Minimum	Maximum	Units
C_{IN}	Input capacitance	–	10	pF

Table 10 • I/O Weak Pull-Up/Pull-Down Resistances for DDRIO I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

	DDRIO I/O Bank				
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
VDDI Domain	Min.	Max.	Min.	Max.	Notes
3.3 V	N/A	N/A	N/A	N/A	–
2.5 V	10.6 K	17.3 K	10.5 K	18.1 K	1, 2
1.8 V	1.11 K	19.3 K	11.2 K	20.9 K	1, 2
1.5 V	10 K	13.4 K	9.99 K	13.4 K	1, 2
1.2 V	10.3 K	14.5 K	10.3 K	14.7 K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

Table 11 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

	MSIO I/O Bank				
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
VDDI Domain	Min.	Max.	Min.	Max.	Notes
3.3 V	9.9 K	14.7 K	10.1 K	15.3 K	–
2.5 V	10.1 K	15.1 K	10.1 K	15.7 K	1, 2
1.8 V	10.4 K	16.2 K	10.4 K	17.3 K	1, 2
1.5 V	10.7 K	17.3 K	10.8 K	18.9 K	1, 2
1.2 V	11.3 K	19.7 K	11.5 K	22.7 K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

Table 12 • I/O Weak Pull-Up/Pull-Down Resistances for MSIOD I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		Notes
	Min.	Max.	Min.	Max.	
3.3 V	N/A	N/A	N/A	N/A	–
2.5 V	9.6 K	14.1 K	9.5 K	13.9 K	1, 2
1.8 V	9.7 K	14.7 K	9.7 K	14.5 K	1, 2
1.5 V	9.9 K	15.3 K	9.8 K	15 K	1, 2
1.2 V	10.3 K	16.7 K	10 K	16.2 K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

Table 13 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value for Schmitt Trigger Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typical, unless otherwise noted)
3.3 V LVTTL / LVCMOS / PCI / PCI-X	0.05 × VDDI (worst-case)
2.5 V LVCMOS	0.05 × VDDI (worst-case)
1.8 V LVCMOS	0.1 × VDDI (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

Single-Ended I/O Standards

Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 SoC FPGAs are LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 14 • LVTTL/LVCMOS 3.3 V DC Voltage Specification

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.4	–	–	V	1
VOL	DC output logic Low		–	–	0.4	V	1
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	

Notes:

1. *The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.*

Table 15 • LVTTL/LVCMOS 3.3 V Minimum and Maximum AC Input and Output Levels

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVTTL/LVCMOS 3.3 V AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	600	Mbps	
LVTTL/LVCMOS 3.3 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	1.4	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 16 • LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications

Output Drive Selection / MSIO I/O Bank	VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	VDDI – 0.4	0.4	2	2	
4 mA	VDDI – 0.4	0.4	4	4	
8 mA	VDDI – 0.4	0.4	8	8	
12 mA	VDDI – 0.4	0.4	12	12	
16 mA	VDDI – 0.4	0.4	16	16	
20 mA	VDDI – 0.4	0.4	20	20	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 17 • LVTTL/LVCMOS 3.3 V Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		–1	Std.	–1	Std.	
LVTTL/LVCMOS 3.3 V (For MSIO I/O bank)	None	2.323	2.734	2.35	2.766	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 18 • LVTTL/LVCMOS 3.3 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVTTL/LVCMOS 3.3 V (for MSIO I/O bank)												
2 mA	Slow	3.192	3.755	3.47	4.083	3.235	3.807	3.572	4.202	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.932	3.45	4.349	5.117	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	4.43	5.212	4.723	5.557	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	5.648	6.645	5.343	6.287	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	5.891	6.931	5.523	6.499	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	6.16	7.248	5.774	6.794	6.262	7.367	5.876	6.913	ns

LVCMOS 2.5 V

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGAs in compliance to the JEDEC specification JESD8-5A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 19 • LVCMOS 2.5 V DC Voltage Specification

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
LVCMOS 2.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		1.7	–	2.625	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		1.7	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.7	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 2.5 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.4	–	–	V	1
VOL	DC output logic Low		–	–	0.4	V	1

Notes:

1. *The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.*

Table 20 • LVCMOS 2.5 V Minimum and Maximum AC Input and Output Levels

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 2.5 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	250	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	410	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	420	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 33, 25, 20		Ohms	
LVCMOS 2.5 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path			1.2		V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})			2K		Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})			5		pF	
Cload	Capacitive loading for data path (t_{DP})			5		pF	

Table 21 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
2 mA	2 mA	2 mA	VDDI – 0.4	0.4	2	2	
4 mA	4 mA	4 mA	VDDI – 0.4	0.4	4	4	
6 mA	6 mA	6 mA	VDDI – 0.4	0.4	6	6	
8 mA	8 mA	8 mA	VDDI – 0.4	0.4	8	8	
12 mA	12 mA	12 mA	VDDI – 0.4	0.4	12	12	
16 mA	N/A	16 mA	VDDI – 0.4	0.4	16	16	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 22 • LVCMOS 2.5 V Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		–1	Std.	–1	Std.	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.88	2.213	1.989	2.342	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.547	2.996	2.556	3.006	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.35	2.765	2.365	2.783	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 23 • LVCMOS 2.5 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 2.5 V (for DDRIO I/O bank with FIXED CODES)												
2 mA	Slow	3.657	4.302	3.738	4.397	3.675	4.323	3.894	4.582	3.563	4.192	ns
	Medium	3.374	3.97	3.479	4.092	3.396	3.995	3.635	4.277	3.284	3.864	ns
	Medium fast	3.239	3.811	3.363	3.956	3.261	3.836	3.519	4.141	3.149	3.705	ns
	Fast	3.224	3.793	3.356	3.947	3.246	3.818	3.512	4.132	3.134	3.687	ns
4 mA	Slow	3.095	3.641	4.582	5.39	4.192	4.931	4.738	5.575	4.348	5.116	ns
	Medium	2.825	3.324	4.336	5.1	3.907	4.596	4.492	5.285	4.063	4.781	ns
	Medium fast	2.701	3.178	4.208	4.95	3.789	4.457	4.364	5.135	3.945	4.642	ns
	Fast	2.69	3.165	4.203	4.944	3.784	4.451	4.359	5.129	3.94	4.636	ns
6 mA	Slow	2.919	3.434	4.929	5.798	4.518	5.315	5.085	5.983	4.674	5.5	ns
	Medium	2.65	3.118	4.689	5.516	4.219	4.963	4.845	5.701	4.375	5.148	ns
	Medium fast	2.529	2.975	4.568	5.373	4.103	4.826	4.724	5.558	4.259	5.011	ns
	Fast	2.516	2.96	4.561	5.365	4.095	4.817	4.717	5.55	4.251	5.002	ns

Table 23 • **LVCMOS 2.5 V Transmitter Characteristics (continued)**

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
8 mA	Slow	2.863	3.368	5.04	5.929	4.6132	5.427	5.196	6.114	4.769	5.612	ns
	Medium	2.599	3.058	4.796	5.642	4.315	5.076	4.952	5.827	4.471	5.261	ns
	Medium fast	2.483	2.921	4.676	5.5	4.208	4.949	4.832	5.685	4.364	5.134	ns
	Fast	2.467	2.902	4.67	5.493	4.192	4.931	4.826	5.678	4.348	5.116	ns
12 mA	Slow	2.747	3.232	5.234	6.157	4.782	5.625	5.39	6.342	4.938	5.81	ns
	Medium	2.493	2.934	5.01	5.893	4.494	5.286	5.166	6.078	4.65	5.471	ns
	Medium fast	2.382	2.803	4.911	5.777	4.39	5.164	5.067	5.962	4.546	5.349	ns
	Fast	2.369	2.787	4.907	5.773	4.382	5.154	5.063	5.958	4.538	5.339	ns
16 mA	Slow	2.677	3.149	5.419	6.375	4.924	5.792	5.575	6.56	5.08	5.977	ns
	Medium	2.432	2.862	5.216	6.135	4.645	5.464	5.372	6.32	4.801	5.649	ns
	Medium fast	2.324	2.734	5.141	6.048	4.544	5.346	5.297	6.233	4.7	5.531	ns
	Fast	2.313	2.721	5.14	6.046	4.543	5.344	5.296	6.231	4.699	5.529	ns
LVCMOS 2.5 V (for MSIO I/O bank)												
2 mA	Slow	3.48	4.095	3.855	4.534	3.785	4.453	3.877	4.56	3.807	4.479	ns
4 mA	Slow	2.583	3.039	4.121	4.849	4.665	5.488	4.143	4.874	4.687	5.513	ns
6 mA	Slow	2.392	2.815	4.887	5.75	5.061	5.955	4.909	5.775	5.083	5.98	ns
8 mA	Slow	2.309	2.717	5.79	6.812	5.501	6.472	5.812	6.837	5.523	6.497	ns
12 mA	Slow	2.333	2.745	6.109	7.188	5.69	6.695	6.131	7.213	5.712	6.72	ns
16 mA	Slow	2.412	2.838	6.518	7.669	5.985	7.042	6.54	7.694	6.007	7.067	ns
LVCMOS 2.5 V (for MSIOD I/O bank)												
2 mA	Slow	2.206	2.596	4.877	5.737	4.682	5.508	4.935	5.805	4.74	5.576	ns
4 mA	Slow	1.835	2.159	5.355	6.3	5.092	5.991	5.413	6.368	5.15	6.059	ns
6 mA	Slow	1.709	2.01	5.755	6.77	5.441	6.401	5.813	6.838	5.499	6.469	ns
8 mA	Slow	1.63	1.918	6.168	7.256	5.758	6.774	6.226	7.324	5.816	6.842	ns
12 mA	Slow	1.648	1.939	6.461	7.601	5.969	7.022	6.519	7.669	6.027	7.09	ns

1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs in compliance to the JEDEC specification JESD8-7A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 24 • **LVCMOS 1.8 V DC Voltage Specification**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.710	1.8	1.89	V	
LVCMOS 1.8 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		0.65 * VDDI	–	1.89	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 1.8 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.45	–	–	V	
VOL	DC output logic Low		–	–	0.45	V	

Table 25 • **LVCMOS 1.8 V Minimum and Maximum AC Input and Output Levels**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.8 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	200	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	295	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	320	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 33, 25, 20		Ohms	
LVCMOS 1.8 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 26 • LVCMOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
2 mA	2 mA	2 mA	VDDI – 0.45	0.45	2	2	
4 mA	4 mA	4 mA	VDDI – 0.45	0.45	4	4	
6 mA	6 mA	6 mA	VDDI – 0.45	0.45	6	6	
8 mA	8 mA	8 mA	VDDI – 0.45	0.45	8	8	
10 mA	10 mA	10 mA	VDDI – 0.45	0.45	10	10	
12 mA	N/A	12 mA	VDDI – 0.45	0.45	12	12	
N/A	N/A	16 mA	VDDI – 0.45	0.45	16	16	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.71 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 27 • LVCMOS 1.8 V Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		–1	Std.	–1	Std.	
LVCMOS 1.8 V (for DDRIO I/O bank)	None	2.025	2.383	2.156	2.538	ns
	50	2.049	2.411	2.286	2.69	ns
	75	2.036	2.395	2.236	2.632	ns
	150	2.035	2.395	2.193	2.58	ns
LVCMOS 1.8 V (for MSIO I/O bank)	None	2.959	3.482	2.944	3.464	ns
	50	3.111	3.661	3.105	3.654	ns
	75	3.06	3.601	3.048	3.587	ns
	150	3.008	3.54	2.994	3.523	ns
LVCMOS 1.8 V (for MSIOD I/O bank)	None	2.671	3.142	2.658	3.128	ns
	50	2.835	3.335	2.835	3.336	ns
	75	2.78	3.271	2.772	3.261	ns
	150	2.726	3.208	2.715	3.194	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 28 • LVCMOS 1.8 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.8 V (for DDRIO I/O bank with FIXED CODES)												
2 mA	Slow	4.234	4.981	4.632	5.45	4.245	4.995	4.908	5.774	4.434	5.216	ns
	Medium	3.824	4.498	4.349	5.117	3.84	4.519	4.625	5.441	4.116	4.843	ns
	Medium fast	3.627	4.267	4.205	4.948	3.708	4.363	4.481	5.272	3.984	4.687	ns
	Fast	3.605	4.241	4.196	4.938	3.697	4.35	4.472	5.262	3.973	4.674	ns
4 mA	Slow	3.923	4.615	5.127	6.032	4.618	5.433	5.403	6.356	4.894	5.757	ns
	Medium	3.518	4.138	4.845	5.701	4.285	5.042	5.121	6.025	4.561	5.366	ns
	Medium fast	3.321	3.907	4.69	5.519	4.15	4.882	4.966	5.843	4.426	5.206	ns
	Fast	3.301	3.883	4.681	5.507	4.141	4.872	4.957	5.831	4.417	5.196	ns
6 mA	Slow	3.71	4.364	5.344	6.288	4.804	5.653	5.62	6.612	5.08	5.977	ns
	Medium	3.333	3.921	5.07	5.965	4.501	5.296	5.346	6.289	4.777	5.62	ns
	Medium fast	3.155	3.712	4.934	5.806	4.381	5.155	5.21	6.13	4.657	5.479	ns
	Fast	3.134	3.688	4.926	5.796	4.372	5.144	5.202	6.12	4.648	5.468	ns
8 mA	Slow	3.619	4.258	5.539	6.517	4.973	5.851	5.815	6.841	5.249	6.175	ns
	Medium	3.246	3.819	5.266	6.196	4.66	5.483	5.542	6.52	4.936	5.807	ns
	Medium fast	3.066	3.607	5.129	6.035	4.535	5.336	5.405	6.359	4.811	5.66	ns
	Fast	3.046	3.584	5.125	6.029	4.527	5.327	5.401	6.353	4.803	5.651	ns
10 mA	Slow	3.498	4.115	5.77	6.789	5.168	6.08	6.046	7.113	5.444	6.404	ns
	Medium	3.138	3.692	5.506	6.479	4.853	5.71	5.782	6.803	5.129	6.034	ns
	Medium fast	2.966	3.489	5.39	6.341	4.737	5.573	5.666	6.665	5.013	5.897	ns
	Fast	2.945	3.464	5.383	6.334	4.727	5.562	5.659	6.658	5.003	5.886	ns
12 mA	Slow	3.417	4.02	5.807	6.832	5.188	6.104	6.083	7.156	5.464	6.428	ns
	Medium	3.076	3.618	5.552	6.532	4.9	5.765	5.828	6.856	5.176	6.089	ns
	Medium fast	2.913	3.427	5.449	6.412	4.796	5.642	5.725	6.736	5.072	5.966	ns
	Fast	2.894	3.405	5.439	6.4	4.788	5.633	5.715	6.724	5.064	5.957	ns
16 mA	Slow	3.366	3.96	5.95	7	5.3	6.236	6.226	7.324	5.576	6.56	ns
	Medium	3.03	3.565	5.705	6.712	5.006	5.89	5.981	7.036	5.282	6.214	ns
	Medium fast	2.87	3.377	5.619	6.611	4.904	5.77	5.895	6.935	5.18	6.094	ns
	Fast	2.853	3.357	5.613	6.605	4.901	5.766	5.889	6.929	5.177	6.09	ns

Table 28 • LVCMOS 1.8 V Transmitter Characteristics (continued)

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.8 V (for MSIO I/O bank)												
2 mA	Slow	3.441	4.047	4.966	5.843	5.213	6.132	4.891	5.755	5.138	6.044	ns
4 mA	Slow	3.218	3.786	5.74	6.753	5.643	6.639	5.665	6.665	5.568	6.551	ns
6 mA	Slow	3.141	3.694	6.662	7.838	6.107	7.184	6.587	7.75	6.032	7.096	ns
8 mA	Slow	3.165	3.723	6.973	8.203	6.291	7.401	6.898	8.115	6.216	7.313	ns
10 mA	Slow	3.202	3.767	7.325	8.617	6.51	7.659	7.25	8.529	6.435	7.571	ns
12 mA	Slow	3.277	3.855	7.467	8.785	6.613	7.78	7.392	8.697	6.538	7.692	ns
LVCMOS 1.8 V (for MSIOD I/O bank)												
2 mA	Slow	2.725	3.206	5.189	6.105	4.982	5.862	5.204	6.123	4.997	5.88	ns
4 mA	Slow	2.242	2.638	5.714	6.722	5.433	6.392	5.729	6.74	5.448	6.41	ns
6 mA	Slow	1.995	2.347	6.357	7.478	5.972	7.025	6.3721	7.496	5.987	7.043	ns
8 mA	Slow	2.001	2.354	6.618	7.786	6.178	7.268	6.633	7.804	6.193	7.286	ns
10 mA	Slow	2.025	2.382	6.925	8.147	6.397	7.526	6.94	8.165	6.412	7.544	ns

1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs in compliance to the JEDEC specification JESD8-11A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 29 • **LVCMOS 1.5 V DC Voltage Specification**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
LVCMOS 1.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)		0.65 * VDDI	–	1.575	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC	Input current Low		–	–	10	µA	
LVCMOS 1.5 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI * 0.75	–	–	V	
VOL	DC output logic Low		–	–	VDDI * 0.25	V	

Table 30 • **LVCMOS 1.5 V Minimum and Maximum AC Input and Output Levels**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.5 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	130	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	80	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	170	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 40		Ohms	
LVCMOS 1.5 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point		–	0.75	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 31 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)			
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	2 mA	2 mA	VDDI * 0.75	VDDI * 0.25	2	2	
4 mA	4 mA	4 mA	VDDI * 0.75	VDDI * 0.25	4	4	
6 mA	6 mA	6 mA	VDDI * 0.75	VDDI * 0.25	6	6	
8 mA	N/A	8 mA	VDDI * 0.75	VDDI * 0.25	8	8	
N/A	N/A	10 mA	VDDI * 0.75	VDDI * 0.25	10	10	
N/A	N/A	12 mA	VDDI * 0.75	VDDI * 0.25	12	12	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.425 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 32 • LVCMOS 1.5 V Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		–1	Std.	–1	Std.	
LVCMOS 1.5 V (for DDRIO I/O bank)	None	2.108	2.481	2.143	2.523	ns
	50	2.175	2.56	2.33	2.741	ns
	75	2.156	2.538	2.255	2.653	ns
	150	2.14	2.519	2.19	2.577	ns
LVCMOS 1.5 V (for MSIO I/O bank)	None	3.372	3.967	3.346	3.936	ns
	50	3.715	4.37	3.684	4.334	ns
	75	3.594	4.227	3.562	4.19	ns
	150	3.476	4.089	3.449	4.057	ns
LVCMOS 1.5 V (for MSIOD I/O bank)	None	3.02	3.553	2.991	3.519	ns
	50	3.359	3.952	3.329	3.917	ns
	75	3.223	3.791	3.189	3.752	ns
	150	3.114	3.664	3.082	3.626	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 33 • LVCMOS 1.5 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.5 V (for DDRIO I/O bank)												
2 mA	Slow	5.122	6.026	4.896	5.76	5.145	6.052	5.258	6.186	4.893	5.756	ns
	Medium	4.58	5.389	4.615	5.429	4.6	5.411	4.977	5.855	4.357	5.126	ns
	Medium fast	4.323	5.086	4.442	5.226	4.341	5.107	4.804	5.652	4.228	4.974	ns
	Fast	4.296	5.054	4.429	5.21	4.314	5.075	4.791	5.636	4.219	4.963	ns

Table 33 • **LVCMOS 1.5 V Transmitter Characteristics (continued)**

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
4 mA	Slow	4.449	5.235	5.696	6.701	5.096	5.995	6.058	7.127	5.458	6.421	ns
	Medium	3.961	4.66	5.416	6.371	4.754	5.592	5.778	6.797	5.116	6.018	ns
	Medium fast	3.729	4.387	5.268	6.198	4.619	5.434	5.63	6.624	4.981	5.86	ns
	Fast	3.704	4.358	5.262	6.191	4.611	5.425	5.624	6.617	4.973	5.851	ns
6 mA	Slow	4.244	4.993	6.028	7.092	5.374	6.322	6.39	7.518	5.736	6.748	ns
	Medium	3.774	4.44	5.752	6.767	5.035	5.924	6.114	7.193	5.397	6.35	ns
	Medium fast	3.554	4.17	5.616	6.607	4.908	5.774	5.978	7.033	5.27	6.2	ns
	Fast	3.519	4.14	5.603	6.591	4.897	5.761	5.965	7.017	5.259	6.187	ns
8 mA	Slow	4.099	4.823	6.222	7.32	5.492	6.462	6.584	7.746	5.854	6.888	ns
	Medium	3.656	4.301	5.949	6.999	5.191	6.107	6.311	7.425	5.553	6.553	ns
	Medium fast	3.437	4.044	5.82	6.847	5.073	5.968	6.182	7.273	5.435	6.394	ns
	Fast	3.41	4.012	5.816	6.843	5.063	5.957	6.178	7.269	5.425	6.383	ns
10 mA	Slow	4.029	4.74	6.37	7.495	5.603	6.592	6.732	7.921	5.965	7.018	ns
	Medium	3.601	4.237	6.111	7.189	5.307	6.243	6.473	7.615	5.669	6.669	ns
	Medium fast	3.384	3.981	5.989	7.045	5.188	6.103	6.351	7.471	5.55	6.529	ns
	Fast	3.357	3.949	5.983	7.038	5.178	6.092	6.345	7.464	5.54	6.518	ns
12 mA	Slow	3.974	4.675	6.48	7.623	5.706	6.713	6.842	8.049	6.068	7.139	ns
	Medium	3.55	4.176	6.222	7.32	5.389	6.34	6.584	7.746	5.751	6.766	ns
	Medium fast	3.345	3.935	6.126	7.207	5.279	6.211	6.488	7.633	5.641	6.637	ns
	Fast	3.316	3.902	6.124	7.204	5.264	6.193	6.486	7.63	5.626	6.619	ns
LVCMOS 1.5 V (for MSIO I/O bank)												
2 mA	Slow	4.423	5.203	5.723	6.733	5.686	6.69	5.609	6.599	5.572	6.556	ns
4 mA	Slow	4.05	4.765	7.472	8.791	6.639	7.811	7.358	8.657	6.525	7.677	ns
6 mA	Slow	4.081	4.801	7.773	9.145	6.823	8.027	7.659	9.011	6.709	7.893	ns
8 mA	Slow	4.234	4.98	8.332	9.802	7.164	8.428	8.218	9.668	7.05	8.294	ns
LVCMOS 1.5 V (for MSIOD I/O bank)												
2 mA	Slow	2.735	3.218	6.025	7.089	5.7	6.706	6.03	7.095	5.705	6.712	ns
4 mA	Slow	2.426	2.854	6.733	7.921	6.923	7.404	6.738	7.927	6.298	7.41	ns
6 mA	Slow	2.433	2.862	7.118	8.374	6.591	7.754	7.123	8.38	6.596	7.76	ns

1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 FPGAs in compliance to the JEDEC specification JESD8-12A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 34 • LVCMOS 1.2 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.14	1.2	1.26	V	
LVCMOS 1.2 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		0.65 * VDDI	–	1.26	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 1.2 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI * 0.75	–	–	V	
VOL	DC output logic Low		–	–	VDDI * 0.25	V	

Table 35 • LVCMOS 1.2 V Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.2 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 2 pF load, maximum drive/slew	–	–	75	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2.5 pF load, maximum drive/slew	–	–	50	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 2.5 pF load, maximum drive/slew	–	–	100	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 40		Ohms	
LVCMOS 1.2 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point		–	0.6	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 36 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)			
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	2 mA	2 mA	VDDI * 0.75	VDDI * 0.25	2	2	
4 mA	4 mA	4 mA	VDDI * 0.75	VDDI * 0.25	4	4	
N/A	N/A	6 mA	VDDI * 0.75	VDDI * 0.25	6	6	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.14 V

AC Switching Characteristics for Receiver (Input Buffers))

Table 37 • LVCMOS 1.2 V Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		
		–1	Std.	–1	Std.	Units
LVCMOS 1.2 V (for DDRIO I/O bank)	None	2.505	2.947	2.523	2.968	ns
	50	2.635	3.1	2.88	3.388	ns
	75	2.547	2.996	2.737	3.22	ns
	150	2.476	2.913	2.617	3.079	ns
LVCMOS 1.2 V (for MSIO I/O bank)	None	4.775	5.617	4.736	5.572	ns
	50	6.729	7.916	6.64	7.811	ns
	75	5.893	6.933	5.821	6.848	ns
	150	5.223	6.144	5.172	6.085	ns
LVCMOS 1.2 V (for MSIOD I/O bank)	None	4.215	4.959	4.175	4.912	ns
	50	6.979	8.211	6.867	8.08	ns
	75	5.674	6.675	5.594	6.581	ns
	150	4.777	5.621	4.718	5.551	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 38 • LVCMOS 1.2 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.2 V (for DDRIO I/O bank)												
2 mA	Slow	6.703	7.897	6.744	7.935	6.723	7.909	7.233	8.51	6.546	7.701	ns
	Medium	5.912	6.955	6.398	7.527	5.915	6.959	6.887	8.102	6.009	7.069	ns
	Medium fast	5.5	6.469	6.183	7.274	5.5	6.471	6.672	7.849	5.835	6.865	ns
	Fast	5.462	6.426	6.157	7.244	5.463	6.427	6.646	7.819	5.828	6.857	ns
4 mA	Slow	6.109	7.186	7.516	8.843	6.544	7.699	8.005	9.418	7.033	8.274	ns
	Medium	5.355	6.299	7.148	8.41	6.183	7.274	7.637	8.985	6.672	7.849	ns
	Medium fast	4.953	5.826	6.951	8.177	6.01	7.071	7.44	8.752	6.499	7.646	ns
	Fast	4.911	5.777	6.938	8.162	5.999	7.057	7.427	8.737	6.488	7.632	ns
6 mA	Slow	5.89	6.929	7.848	9.233	6.826	8.03	8.337	9.808	7.315	8.605	ns
	Medium	5.176	6.089	7.497	8.819	6.454	7.593	7.986	9.394	6.943	8.168	ns
	Medium fast	4.792	5.637	7.319	8.611	6.286	7.395	7.808	9.186	6.775	7.97	ns
	Fast	4.754	5.593	7.288	8.574	6.28	7.388	7.777	9.149	6.769	7.963	ns
LVCMOS 1.2 V (for MSIO I/O bank)												
2 mA	Slow	6.746	7.937	10.07	11.848	8.596	10.114	9.867	11.608	8.393	9.874	ns
4 mA	Slow	7.068	8.315	11.189	13.164	9.246	10.878	10.986	12.924	9.043	10.638	ns

Table 38 • **LVCMOS 1.2 V Transmitter Characteristics (continued)**

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.2 V (for MSIOD I/O bank)												
2 mA	Slow	3.883	4.568	7.975	9.382	7.508	8.833	7.994	9.404	7.527	8.855	ns
4 mA	Slow	3.774	4.44	8.953	10.533	8.296	9.76	8.972	10.555	8.315	9.782	ns

3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 39 • PCI/PCI-X DC Voltage Specification – Applicable to MSIO Bank ONLY

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
PCI/PCIX Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
PCI/PCIX DC Input Voltage Specification							
VI	DC input voltage		0	–	3.45	V	
IIH(DC)	Input current High		–	–	10	µA	
IIL(DC)	Input current Low		–	–	10	µA	
PCI/PCIX DC Output Voltage Specification							
VOH	DC output logic High		Per PCI Specification			V	
VOL	DC output logic Low		Per PCI Specification			V	

Table 40 • PCI/PCI-X Minimum and Maximum AC Input and Output Levels – Applicable to MSIO Bank ONLY

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
PCI/PCI-X AC Specifications							
Fmax	Maximum data rate (MSIO I/O bank)	AC Loading: per JEDEC specifications	–	–	630	Mbps	
PCI/PCI-X AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path (falling edge)		–	0.615 * VDDI	–	V	
Vtrip	Measuring/trip point for data path (rising edge)		–	0.285 * VDDI	–	V	
Rtt_test	Resistance for data test path		–	25	–	Ohms	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 41 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		–1	Std.	–1	Std.	
PCI/PCIX (for MSIO I/O bank)	None	2.29	2.694	2.299	2.704	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 42 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
PCI/PCIX (for MSIO I/O bank)											
	2.146	2.525	5.97	7.024	5.433	6.392	6.095	7.171	5.558	6.539	ns

Memory Interface and Voltage Referenced I/O Standards

High-Speed Transceiver Logic (HSTL)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 43 • **HSTL DC Voltage Specification**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
VTT	Termination voltage		0.698	0.750	0.803	V	
VREF	Input reference voltage		0.698	0.750	0.803	V	
HSTL DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.1	–	1.575	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.1	V	
IIH (DC)	Input current High		–	–	10	V	
IIL (DC)	Input current Low		–	–	10	V	
HSTL DC Output Voltage Specification							
HSTL Class I							
VOH	DC output logic High		VDDI – 0.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
IOH at VOH	Output minimum source DC current (MSIOD I/O bank)		–7.8	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIOD I/O bank)		7.8	–	–	mA	1
IOH at VOH	Output minimum source DC current (MSIO and DDRIO I/O banks)		–8.0	–	–	mA	
IOL at VOL	Output minimum sink current (MSIO and DDRIO I/O banks)		8.0	–	–	mA	
HSTL Class II (Applicable to DDRIO I/O Bank Only)							
VOH	DC output logic High		VDDI – 0.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
IOH at VOH	Output minimum source DC current		–16.0	–	–	mA	
IOL at VOL	Output minimum sink current		16.0	–	–	mA	
HSTL DC Differential Voltage Specifications							
VID (DC)	DC input differential voltage		0.2	–	–	V	

Notes:

1. *MSIOD I/O bank HSTL Class I does not meet standard JEDEC test point. Use provided lower current values as specified.*

Table 44 • HSTL Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
HSTL AC Differential Voltage Specifications							
VDIFF (AC)	AC input differential voltage		0.4	–	–	V	
Vx (AC)	AC differential cross point voltage		0.68	–	0.9	V	
HSTL AC Specifications							
Fmax	Maximum data rate (DDRIO I/O bank)	AC loading: per JEDEC specifications	–	–	800	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 3 pF / 50 Ohm load	–	–	140	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 3 pF / 50 Ohm load	–	–	180	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistance = 191 Ohms	–	25.5, 47.8	–	Ohms	
RTT	Effective impedance value (with respect to reference resistor of 191 Ohms) (ODT for DDRIO I/O bank only)	Reference resistance = 191 Ohms	–	47.8	–	Ohms	
RTT	Effective impedance value (ODT for MSIO and MSIOD I/O banks only)	Reference resistance = 191 Ohms	–	50, 75, 150	–	Ohms	
HSTL AC Test Parameters Specification							
Vtrip	Measuring/trip point for data path		–	0.75	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Rtt_test	Reference resistance for data test path for SSTL15 Class I (t_{DP})			50		Ohms	
Rtt_test	Reference resistance for data test path for SSTL15 Class II (t_{DP})		–	25	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 45 • HSTL Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
HSTL (for DDRIO I/O bank)				
Pseudo differential	None	1.662	1.956	ns
	47.8	1.671	1.966	ns
True differential	None	1.68	1.976	ns
	47.8	1.686	1.983	ns
HSTL (for MSIO I/O bank)				
Pseudo differential	None	7.345	8.641	ns
	50	6.736	7.924	ns
	75	6.965	8.194	ns
	150	7.157	8.42	ns
True differential	None	7.325	8.617	ns
	50	7.258	8.538	ns
	75	7.334	8.628	ns
	150	7.433	8.628	ns
HSTL (for MSIOD I/O bank)				
Pseudo differential	None	6.353	7.474	ns
	50	6.042	7.108	ns
	75	6.113	7.192	ns
	150	6.237	7.337	ns
True differential	None	6.568	7.727	ns
	50	6.577	7.737	ns
	75	6.576	7.736	ns
	150	6.62	7.788	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 46 • HSTL Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	Units
HSTL Class I											
For DDRIO I/O Bank											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.505	2.947	2.505	2.947	ns
Differential	2.621	3.083	2.937	3.456	2.935	3.454	2.925	3.442	2.923	3.44	ns
For MSIO I/O Bank											
Single-ended	3.859	4.539	3.422	4.027	3.392	3.991	3.308	3.893	3.278	3.857	ns
Differential	4.006	4.713	4.04	4.752	4.03	4.741	3.931	4.625	3.921	4.614	ns
For MSIOD I/O Bank											
Single-ended	2.207	2.596	2.252	2.65	2.241	2.636	2.257	2.656	2.246	2.642	ns
Differential	2.37	2.788	2.659	3.128	2.646	3.113	2.665	3.135	2.652	3.12	ns
HSTL Class II											
For DDRIO I/O Bank											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.479	2.916	2.481	2.919	ns
Differential	2.528	2.974	2.909	3.423	2.908	3.422	2.897	3.409	2.896	3.408	ns

Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 devices. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 devices and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 47 • **DDR1/SSTL2 DC Voltage Specification**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
VTT	Termination voltage		1.164	1.250	1.339	V	
VREF	Input reference voltage		1.164	1.250	1.339	V	
DDR/SSTL2 DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.15	–	2.625	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.15	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Lo		–	–	10	µA	
DDR/SSTL2 DC Output Voltage Specification							
SSTL2 Class I (DDR Reduced Drive)							
VOH	DC output logic High		VTT + 0.608	–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.608	V	
IOH at VOH	Output minimum source DC current		8.1	–	–	mA	
IOL at VOL	Output minimum sink current		–8.1	–	–	mA	
SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Banks ONLY							
VOH	DC output logic High		VTT + 0.81	–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.81	V	
IOH at VOH	Output minimum source DC current		16.2	–	–	mA	
IOL at VOL	Output minimum sink current		–16.2	–	–	mA	
SSTL2 DC Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.3	–	–	V	

Table 48 • DDR1/SSTL2 Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL2 AC Differential Voltage Specification							
VDIFF (AC)	AC input differential voltage		0.7	–	–	V	
Vx (AC)	AC differential cross point voltage		0.5 * VDDI – 0.2	–	0.5 * VDDI + 0.2	V	
SSTL2 AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specifications	–	–	400	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 50 Ohm load	–	–	575	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 30 pF / 50 Ohm load	–	–	700	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistor = 150 Ohms	–	20, 42	–	Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	1.25	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Rs	Series resistance for data test path (t_{DP})		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL2 Class I (t_{DP})		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL2 Class II (t_{DP})		–	25	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 49 • DDR1/SSTL2 Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
SSTL2 (for DDRIO I/O bank)				
Pseudo differential	None	1.606	1.889	ns
True differential	None	1.647	1.937	ns
SSTL2 (for MSIO I/O bank)				
Pseudo differential	None	2.859	3.365	ns
True differential	None	2.794	3.286	ns
SSTL2 (for MSIOD I/O bank)				
Pseudo differential	None	2.537	2.985	ns
True differential	None	2.535	2.983	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 50 • DDR1/SSTL2 Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		
	–1	STD	–1	STD	–1	STD	–1	STD	–1	STD	Units
SSTL2 Class I											
For DDRIO I/O Bank											
Single-ended	2.26	2.66	2.107	2.479	2.102	2.472	2.135	2.512	2.13	2.505	ns
Differential	2.26	2.658	2.368	2.786	2.367	2.785	2.393	2.815	2.392	2.814	ns
For MSIO I/O Bank											
Single-ended	2.055	2.417	2.064	2.429	2.057	2.421	2.068	2.433	2.061	2.425	ns
Differential	2.192	2.58	2.434	2.864	2.425	2.852	2.441	2.872	2.432	2.86	ns
For MSIOD I/O Bank											
Single-ended	1.512	1.779	1.624	1.91	1.62	1.909	1.676	1.972	1.676	1.971	ns
Differential	1.676	1.971	1.802	2.119	1.793	2.109	1.854	2.181	1.845	2.171	ns
SSTL2 Class II											
For DDRIO I/O Bank											
Single-ended	2.122	2.497	2.033	2.391	2.028	2.385	2.061	2.424	2.056	2.418	ns
Differential	2.127	2.501	2.338	2.751	2.34	2.752	2.363	2.78	2.365	2.781	ns
For MSIO I/O Bank											
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.991	2.342	1.981	2.33	ns
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.311	2.719	2.304	2.71	ns

Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 devices, and also comply with the reduced and full drive double date rate (DDR2) standard. IGLOO2 FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 51 • SSTL18 DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	
VTT	Termination voltage		0.838	0.900	0.964	V	
VREF	Input reference voltage		0.838	0.900	0.964	V	
SSTL18 DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.125	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.125	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
SSTL18 DC Output Voltage Specification							
SSTL18 Class I (DDR2 Reduced Drive)							
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT– 0.603	V	
IOH at VOH	Output minimum source DC current (MSIO I/O bank only)		4.7	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIO I/O bank only)		–4.7	–	–	mA	1
IOH at VOH	Output minimum source DC current (MSIOD I/O bank only)		6.3	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIOD I/O bank only)		–6.3	–	–	mA	1
IOH at VOH	Output minimum source DC current (DDRIO I/O bank only)		6.5	–	–	mA	1
IOL at VOL	Output minimum sink current (DDRIO I/O bank only)		–6.5	–	–	mA	1

Notes:

1. *MSIO I/O bank SSTL18/DDR2 reduced drive does not have a standard test point. This is defined to fit within the DDR2 reduced drive I/V curve minimums.*
2. *MSIO I/O bank SSTL18/DDR2 Class II does not meet the standard JEDEC test points. Use provided lower current values as specified.*

Table 51 • **SSTL18 DC Voltage Specification (continued)**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
STL18 Class II (DDR2 Full Drive) – Applicable to MSIO and DDRIO I/O Banks ONLY							
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT– 0.603	V	
IOH at VOH	Output minimum source DC current (MSIO I/O bank only)		9.3	–	–	mA	
IOL at VOL	Output minimum sink current (MSIO I/O bank only)		–9.3	–	–	mA	
IOH at VOH	Output minimum source DC current (DDRIO I/O bank only)		13.4	–	–	mA	
IOL at VOL	Output minimum sink current (DDRIO I/O bank only)		–13.4	–	–	mA	
SSTL18 DC Differential Voltage Specification							
VID (DC	DC input differential voltage		0.3	–	–	V	

Notes:

1. *MSIO I/O bank SSTL18/DDR2 reduced drive does not have a standard test point. This is defined to fit within the DDR2 reduced drive I/V curve minimums.*
2. *MSIO I/O bank SSTL18/DDR2 Class II does not meet the standard JEDEC test points. Use provided lower current values as specified.*

Table 52 • SSTL18 Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL18 AC Differential Voltage Specification							
VDIFF (AC)	AC input differential voltage		0.7	–	–	V	
Vx (AC)	AC differential cross point voltage		0.5 * VDDI – 0.175	–	0.5 * VDDI + 0.175	V	
SSTL18 AC Specification							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specification	–	–	800	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 3 pF / 25 Ohm load	–	–	432	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 3 pF / 25 Ohm load	–	–	430	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistor = 150 Ohms	–	20, 42	–	Ohms	
RTT	Effective impedance value (with respect to reference resistor 150 Ohms) (ODT for DDRIO I/O bank only)	Reference resistor = 150 Ohms	–	50, 75, 150	–	Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Rs	Series resistance for data test path (t_{DP})		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL18 Class I (t_{DP})		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL18 Class II (t_{DP})		–	25	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.71 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 53 • DDR2/SSTL18 Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		Units
		–1	STD	
SSTL18 (for DDRIO I/O bank)				
Pseudo differential	None	1.624	1.912	ns
	50	1.63	1.919	ns
	75	1.628	1.917	ns
	150	1.626	1.914	ns
True differential	None	1.646	1.936	ns
	50	1.651	1.942	ns
	75	1.647	1.938	ns
	150	1.643	1.938	ns
SSTL18 (for MSIO I/O bank)				
Pseudo differential	None	4.189	4.928	ns
	50	3.798	4.467	ns
	75	3.941	4.637	ns
	150	4.078	4.797	ns
True differential	None	4.309	5.07	ns
	50	4.288	5.045	ns
	75	4.312	5.073	ns
	150	4.338	5.104	ns
SSTL18 (for MSIOD I/O bank)				
Pseudo differential	None	3.666	4.313	ns
	50	3.568	4.198	ns
	75	3.567	4.197	ns
	150	3.622	4.261	ns
True differential	None	3.834	4.511	ns
	50	3.822	4.496	ns
	75	3.834	4.511	ns
	150	3.857	4.538	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 54 • DDR2/SSTL18 Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		
	–1	STD	–1	STD	–1	STD	–1	STD	–1	STD	Units
SSTL18 Class I											
For DDRIO I/O Bank											
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.241	2.636	2.24	2.635	ns
Differential	2.413	2.84	2.797	3.29	2.797	3.29	2.805	3.3	2.805	3.3	ns
For MSIO I/O Bank											
Single-ended	2.712	3.19	2.767	3.256	2.751	3.237	2.692	3.168	2.676	3.149	ns
Differential	2.849	3.352	3.304	3.887	3.293	3.874	3.233	3.803	3.222	3.79	ns
For MSIOD I/O Bank											
Single-ended	1.839	2.163	1.932	2.273	1.927	2.267	1.947	2.291	1.942	2.285	ns
Differential	2.014	2.369	2.207	2.597	2.198	2.587	2.23	2.615	2.214	2.605	ns
SSTL18 Class II											
For DDRIO I/O Bank											
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.207	2.597	2.206	2.596	ns
Differential	2.315	2.724	2.698	3.173	2.698	3.173	2.706	3.183	2.706	3.183	ns
For MSIO I/O Bank											
Single-ended	3.061	3.601	2.696	3.171	2.673	3.144	2.621	3.083	2.598	3.056	ns
Differential	3.201	3.767	3.141	3.696	3.131	3.684	3.07	3.612	3.06	3.6	ns

Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO2 devices, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 55 • **SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
VTT	Termination voltage		0.698	0.750	0.803	V	
VREF	Input reference voltage		0.698	0.750	0.803	V	
SSTL15 DC Input Voltage Specification							
VIH(DC)	DC input logic High		VREF + 0.1	–	1.575	V	
VIL(DC)	DC input logic Low		–0.3	–	VREF – 0.1	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
SSTL15 DC Output Voltage Specification							
DDR3/SSTL15 Class I (DDR3 Reduced Drive)							
VOH	DC output logic High		0.8 * VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.2 * VDDI	V	
IOH at VOH	Output minimum source DC current		6.5	–	–	mA	
IOL at VOL	Output minimum sink current		–6.5	–	–	mA	
SSTL15 Class II (DDR3 Full Drive)							
VOH	DC output logic High		0.8 * VDDI	–	–	V	
VOL	DC output logic Low		–	-	0.2 * VDDI	V	
IOH at VOH	Output minimum source DC current		7.6	–	–	mA	
IOL at VOL	Output minimum sink current		–7.6	–	–	mA	
SSTL15 Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.2	–	–	V	

Table 56 • **SSTL15 Minimum and Maximum AC Input and Output Levels (for DDRIO I/O Bank Only)**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL15 Differential Voltage Specification							
VDIFF (AC)	AC input differential voltage		0.7	–	–	V	
Vx (AC)	AC differential cross point voltage		0.5 * VDDI – 0.150	–	0.5 * VDDI + 0.150	V	
SSTL15 AC Specification							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specifications			800	Mbps	
Rref	Supported output driver calibrated impedance	Reference resistor = 240 Ohms		34, 40		Ohms	
RTT	Effective impedance value (with respect to reference resistor 240 ohms) (ODT for DDRIO I/O bank only)	Reference resistor = 240 Ohms		20, 30, 40, 60, 120		Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.75	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Rs	Series resistance for data test path (t_{DP})		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL15 Class I (t_{DP})		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL15 Class II (t_{DP})		–	25	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.425 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 57 • DDR3/SSTL15 Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
DDR3/SSTL15 (for DDRIO I/O bank)				
Pseudo differential	None	1.662	1.956	ns
	20	1.673	1.969	ns
	30	1.67	1.965	ns
	40	1.668	1.963	ns
	60	1.666	1.961	ns
	120	1.664	1.958	ns
True differential	None	1.681	1.977	ns
	20	1.695	1.993	ns
	30	1.688	1.985	ns
	40	1.684	1.981	ns
	60	1.68	1.977	ns
	120	1.677	1.972	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 58 • DDR3/SSTL15 Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	STD	–1	STD	–1	STD	–1	STD	–1	STD	
DDR3 Reduced Drive/SSTL15 Class I											
For DDRIO I/O Bank											
Single-ended	2.533	2.98	2.522	2.967	2.523	2.968	2.513	2.956	2.514	2.957	ns
Differential	2.555	3.005	3.073	3.615	3.073	3.615	3.061	3.601	3.601	3.601	ns
DDR3 Full DriveSSTL15 Class II											
For DDRIO I/O Bank											
Single-ended	2.53	2.977	2.514	2.958	2.516	2.96	2.505	2.947	2.507	2.949	ns
Differential	2.552	3.002	2.894	3.405	2.893	3.404	2.882	3.391	2.881	3.39	ns

Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 59 • LPDDR DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	
VTT	Termination voltage		0.838	0.900	0.964	V	
VREF	Input reference voltage		0.838	0.900	0.964	V	
LPDDR DC Input Voltage Specification							
VIH (DC)	DC input logic High		0.7 * VDDI	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	0.3 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LPDDR DC Output Voltage Specification							
VOH	DC output logic High		0.9 * VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.1 * VDDI	V	
IOH at VOH	Output minimum source DC current		0.1	–	–	mA	
IOL at VOL	Output minimum sink current		–0.1	–	–	mA	
LPDDR Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.4 * VDDI	–	–	V	
VDIFF (AC)	AC input differential voltage		0.6 * VDDI			V	
Vx (AC)	AC differential cross point voltage		0.4 * VDDI	–	0.6 * VDDI	V	

Table 60 • LPDDR Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LPDDR AC Specifications							
Fmax	Maximum data rate	AC loading: per JEDEC specifications				Mbps	
Rref	Supported output driver calibrated impedance	Reference resistor = 150 Ohms		20, 42		Ohms	
Rtt	Effective impedance value – ODT	Reference resistor = 150 Ohms		50, 70, 150		Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Rs	Series resistance for data test path (t_{DP})		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for LPDDR (t_{DP})		–	50	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	Ohms	

AC Switching Characteristics

Table 61 • LPDDR Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
LPDDR (for DDRIO I/O Bank)				
Pseudo differential	None	1.625	1.913	ns
	50	1.631	1.92	ns
	75	1.629	1.918	ns
	150	1.627	1.915	ns
True differential	None	1.646	1.936	ns
	50	1.651	1.942	ns
	75	1.647	1.938	ns
	150	1.643	1.933	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 62 • LPDDR Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LPDDR Reduced Drive											
For DDRIO I/O Bank											
Single-ended	2.383	2.804	2.23	2.623	2.29	2.622	2.241	2.636	2.24	2.635	ns
Differential	2.396	2.819	2.764	3.252	2.764	3.252	2.772	3.261	2.772	3.261	ns
LPDDR Full Drive											
For DDRIO I/O Bank											
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.207	2.597	2.206	2.596	ns
Differential	2.298	2.703	2.585	3.041	2.585	3.041	2.593	3.051	2.593	3.051	ns

Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

Table 63 • LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage	2.5 V range	2.375	2.5	2.625	V	
VDDI	Supply voltage	3.3 V range	3.15	3.3	3.45	V	
LVDS DC Input Voltage Specification							
VI	DC Input voltage	2.5 V range	0	–	2.925	V	
VI	DC input voltage	3.3 V range	0	–	3.45	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
LVDS Differential Voltage Specification							
VOD	Differential output voltage swing		250	350	450	mV	
VOCM	Output common mode voltage		1.125	1.25	1.375	V	
VICM	Input common mode voltage		0.05	1.25	1.375	V	
VID	Input differential voltage		100	350	600	mV	

Table 64 • LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	535	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – no pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – minimum pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Fmax	Maximum data rate (for MSIOD I/O Bank) – medium pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Rt	Termination resistance		–	100	–	Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

LVDS25 AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 65 • LVDS25 Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
LVDS (for MSIO I/O bank)	None	2.835	3.334	ns
	100	2.835	3.334	ns
LVDS (for MSIOD I/O bank)	None	2.614	3.075	ns
	100	2.609	3.07	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 66 • LVDS25 Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVDS (for MSIO I/O bank)	2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns
LVDS (for MSIOD I/O bank)											
No pre-emphasis	1.61	1.893	1.844	2.169	1.813	2.133	1.897	2.231	1.866	2.195	ns
Min. pre-emphasis	1.527	1.796	1.852	2.179	1.823	2.145	1.905	2.241	1.876	2.207	ns
Med. pre-emphasis	1.496	1.76	1.861	2.19	1.831	2.154	1.914	2.252	1.884	2.216	ns

LVDS33 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 67 • LVDS33 Receiver Characteristics

	On Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
LVDS33 (for MSIO I/O bank)	None	2.633	3.096	ns
	100	2.63	3.094	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 68 • LVDS33 Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVDS33 (for MSIO I/O bank)	1.942	2.284	1.98	2.33	1.97	2.318	2.029	2.387	2.019	2.375	ns

B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 69 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
Bus LVDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
Bus LVDS DC Output Voltage Specification (for MSIO I/O Bank ONLY)							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
Bus LVDS Differential Voltage Specification							
VOD	Differential output voltage swing (for MSIO I/O bank ONLY)		240	–	460	mV	
VOCM	Output common mode voltage (for MSIO I/O bank ONLY)		1.1	–	1.5	V	
VICM	Input common mode voltage		0.05	–	2.4 – VID/2	V	
VID	Input differential voltage		100	–	2 * VDDI	mV	

Table 70 • B-LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Bus LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	500	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank, receiver ONLY)		–	–	–	Mbps	
Rt	Termination resistance		–	27	–	Ohms	
Bus LVDS AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 71 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
Bus-LVDS (for MSIO I/O Bank)	None	2.798	3.291	ns
	100	2.795	3.288	ns
Bus-LVDS (for MSIOD I/O Bank)	None	2.555	3.005	ns
	100	2.555	3.006	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 72 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	Units
Bus-LVDS (for MSIO I/O Bank)	2.258	2.656	2.343	2.756	2.329	2.74	2.35	2.764	2.336	2.748	ns

M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum Input and Output Levels

Table 73 • M-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
M-LVDS Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
M-LVDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
M-LVDS DC Output Voltage Specification (for MSIO I/O Bank ONLY)							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
M-LVDS Differential Voltage Specification							
VOD	Differential output voltage Swing (for MSIO I/O bank ONLY)		480	–	650	mV	
VOCM	Output common mode voltage (for MSIO I/O bank ONLY)		0.3	–	2.1	V	
VICM	Input common mode voltage		0.3	–	1.2	V	
VID	Input differential voltage		50	–	2400	mV	

Table 74 • M-LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
M-LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	500	Mbps	
Rt	Termination resistance		–	50	–	Ohms	
M-LVDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 75 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
M-LVDS (for MSIO I/O bank)	None	2.798	3.291	ns
	100	2.795	3.288	ns
M-LVDS (for MSIOD I/O bank)	None	2.555	3.005	ns
	100	2.555	3.006	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 76 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
M-LVDS (for MSIO I/O bank)	2.258	2.656	2.348	2.762	2.334	2.746	2.355	2.77	2.341	2.754	ns

Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 77 • Mini-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
Mini-LVDS DC Input Voltage Specification							
VI	DC Input voltage		0	–	2.925	V	
Mini-LVDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
Mini-LVDS Differential Voltage Specification							
VOD	Differential output voltage swing		300	–	600	mV	
VOCM	Output common mode voltage		1	–	1.4	V	
VICM	Input common mode voltage		0.3	–	1.2	V	
VID	Input differential voltage		200	–	600	mV	

Table 78 • Mini-LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Mini-LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	520	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank, No pre-emphasis)	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Min. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Med. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Max. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Rt	Termination resistance		50		150	Ohms	
Mini-LVDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 79 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
Mini-LVDS (for MSIO I/O bank)	None	2.916	3.43	ns
	100	2.911	3.424	ns
Mini-LVDS (for MSIOD I/O bank)	None	2.662	3.133	ns
	100	2.657	3.127	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 80 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
Mini-LVDS (for MSIO I/O bank)	2.097	2.467	2.308	2.715	2.296	2.701	2.315	2.723	2.303	2.709	ns
Mini-LVDS (for MSIOD I/O Bank)											
No pre-emphasis	1.614	1.899	1.562	1.837	1.553	1.826	1.614	1.899	1.605	1.888	ns
Min. pre-emphasis	1.604	1.887	1.839	2.163	1.808	2.127	1.892	2.225	1.861	2.189	ns
Med. pre-emphasis	1.521	1.79	1.847	2.173	1.815	2.135	1.9	2.235	1.868	2.197	ns
Max. pre-emphasis	1.492	1.754	1.857	2.185	1.823	2.144	1.91	2.247	1.876	2.206	ns

RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

Minimum and Maximum Input and Output Levels

Table 81 • RSDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
RSDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
RSDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
RSDS Differential Voltage Specification							
VOD	Differential output voltage swing		100	–	600	mV	
VOCM	Output common mode voltage		0.5	–	1.5	V	
VICM	Input common mode voltage		0.3	–	1.5	V	
VID	Input differential voltage		100	–	2 * VDDI	mV	

Table 82 • RSDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
RSDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	520	Mbps	
Fmax	Maximum data Rate (for MSIOD I/O banks, No pre-emphasis)	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Min. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Med. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Max. pre-emphasis)	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Rt	Termination resistance			100		Ohms	
AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 83 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
RSDS (for MSIO I/O bank)	None	2.916	3.43	ns
	100	2.911	3.424	ns
RSDS (for MSIOD I/O bank)	None	2.662	3.133	ns
	100	2.657	3.127	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 84 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
RSDS (for MSIO I/O bank)	2.097	2.467	2.303	2.709	2.291	2.695	2.31	2.717	2.298	2.703	ns
RSDS (for MSIOD I/O bank)											
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.611	1.896	1.602	1.885	ns
Min. pre-emphasis	1.604	1.887	1.836	2.16	1.805	2.123	1.889	2.222	1.858	2.185	ns
Med. pre-emphasis	1.521	1.79	1.847	2.173	1.815	2.135	1.9	2.235	1.868	2.197	ns
Max. pre-emphasis	1.492	1.754	1.857	2.185	1.823	2.144	1.91	2.247	1.876	2.206	ns

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 devices support only LVPECL receivers and do not support LVPECL transmitters.

Minimum and Maximum Input and Output Levels

Table 85 • LVPECL DC Voltage Specification – Applicable to MSIO I/O Banks Only

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
LVPECL DC Input Voltage Specification							
VIH (DC)	DC input logic High		–	–	2.3	V	
VIL (DC)	DC input logic Low		1.6	–	–	V	
LVPECL Differential Voltage Specification							
VICM	Input common mode voltage		0.3		2.8	V	
VIDIFF	Input differential voltage		100	300	1,000	mV	

Table 86 • LVPECL Minimum and Maximum AC Input and Output Levels – Applicable to MSIO I/O Banks Only

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVPECL AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)		–	–	900	Mbps	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 87 • LVPECL Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		Units
		–1	Std.	
LVPECL (for MSIO I/O bank)	None	2.535	2.983	ns
	100	1.647	1.937	ns

I/O Register Specifications

Input Register

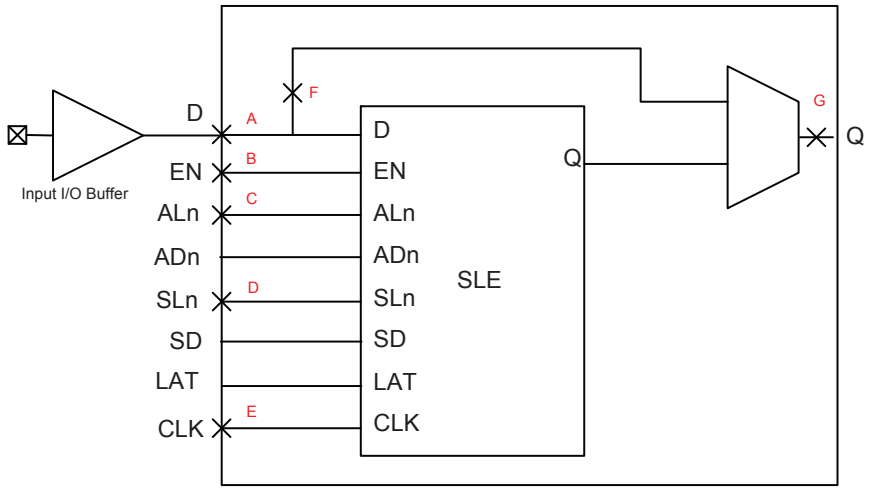


***Figure 3* • Timing Model for Input Register**

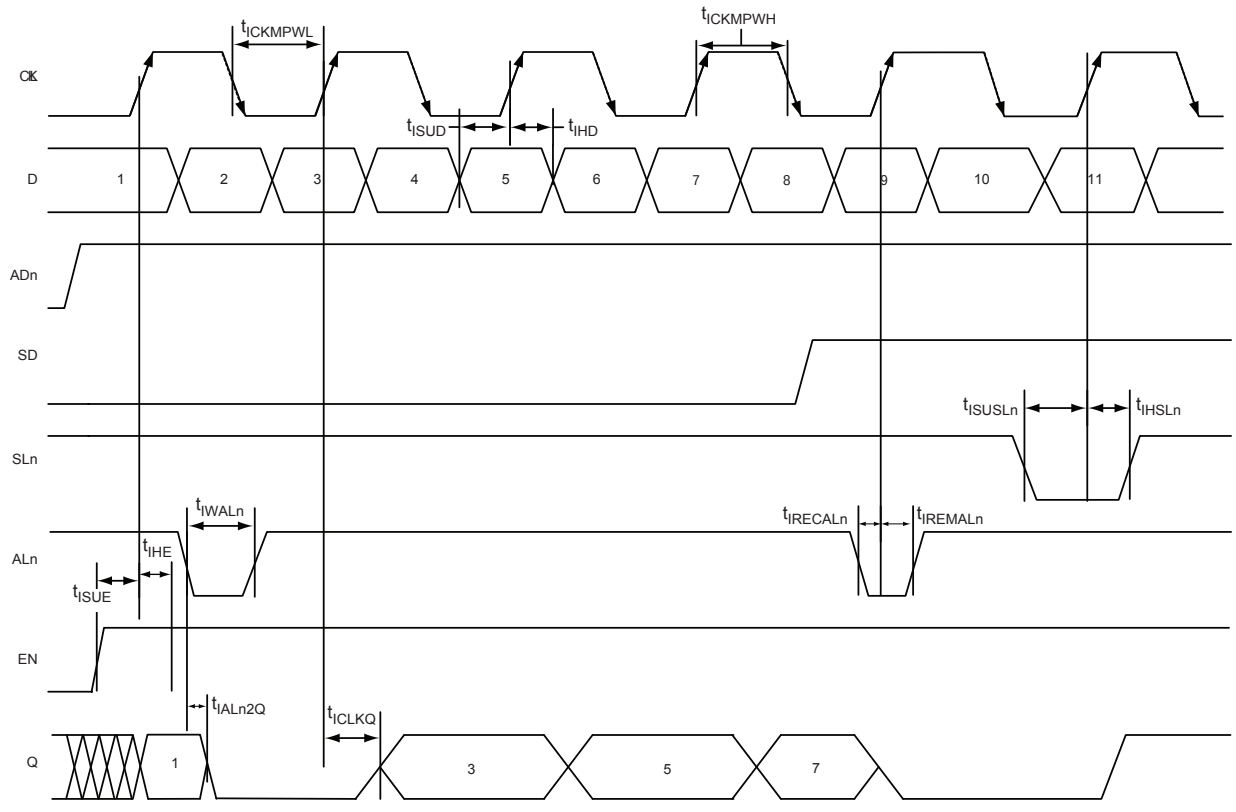


***Figure 4* • I/O Register Input Timing Diagram**

Table 88 • Input Data Enable Register Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	–1	Std.	Units
t_{IBYP}	Bypass Delay of the Input Register	F, G	0.371	0.437	ns
t_{ICLKQ}	Clock-to-Q of the Input Register	E, G	0.168	0.198	ns
t_{ISUD}	Data Setup Time for the Input Register	A, E	0.376	0.443	ns
t_{IHD}	Data Hold Time for the Input Register	A, E	0	0	ns
t_{ISUE}	Enable Setup Time for the Input Register	B, E	0.485	0.57	ns
t_{IHE}	Enable Hold Time for the Input Register	B, E	0	0	ns
t_{ISUSL}	Synchronous Load Setup Time for the Input Register	D, E	0.485	0.57	ns
t_{IHSL}	Synchronous Load Hold Time for the Input Register	D, E	0	0	ns
t_{IALn2Q}	Asynchronous Clear-to-Q of the Input Register (ADn=1)	C, G	0.658	0.774	ns
	Asynchronous Preset-to-Q of the Input Register (ADn=0)	C, G	0.618	0.727	ns
$t_{IREMALn}$	Asynchronous Load Removal Time for the Input Register	C, E	0	0	ns
$t_{IRECALn}$	Asynchronous Load Recovery Time for the Input Register	C, E	0.078	0.091	ns
t_{IWALn}	Asynchronous Load Minimum Pulse Width for the Input Register	C, C	0.32	0.376	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Register	E, E	0.079	0.093	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Register	E, E	0.168	0.197	ns

*Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 7 on page 15 for derating values.*

Output/Enable Register

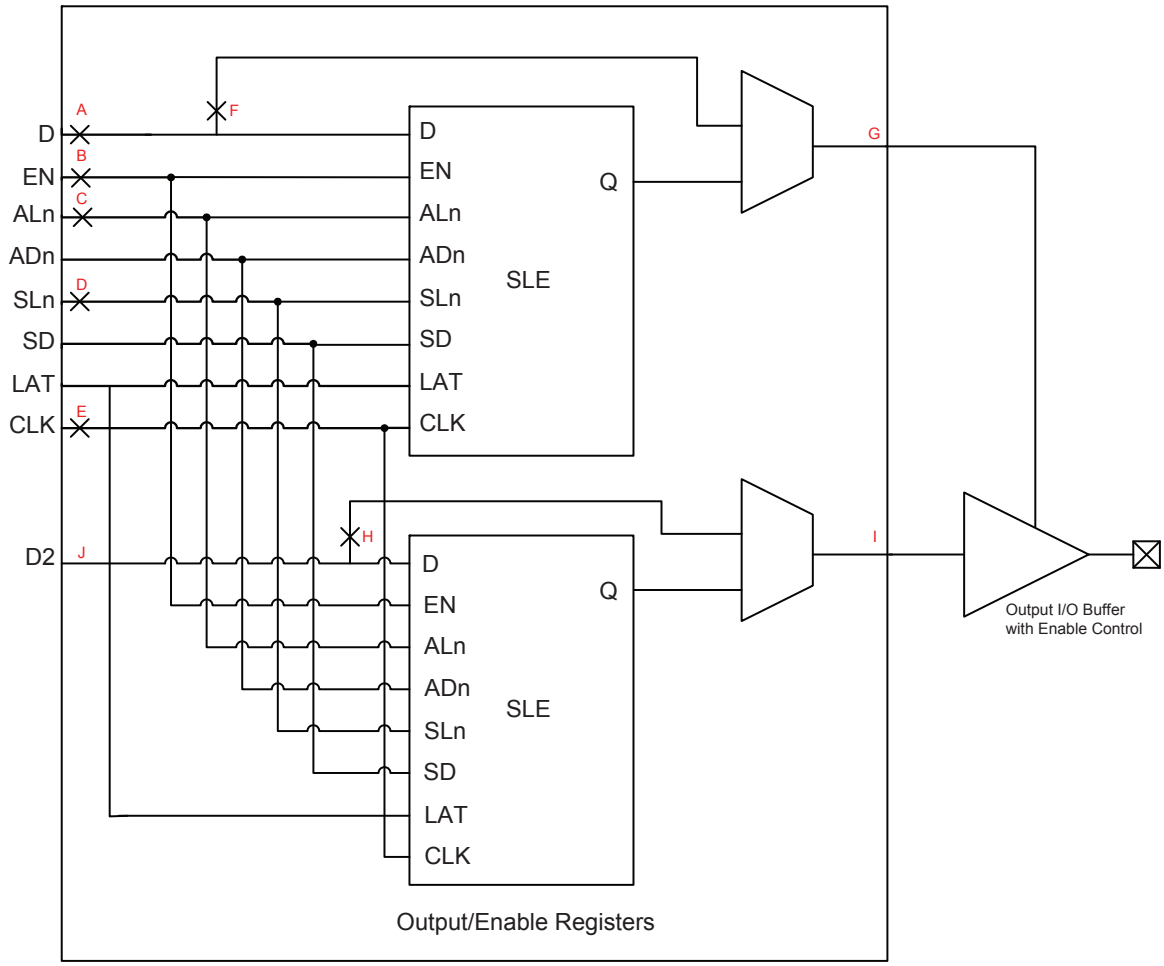


***Figure 5* • Timing Model for Output/Enable Register**

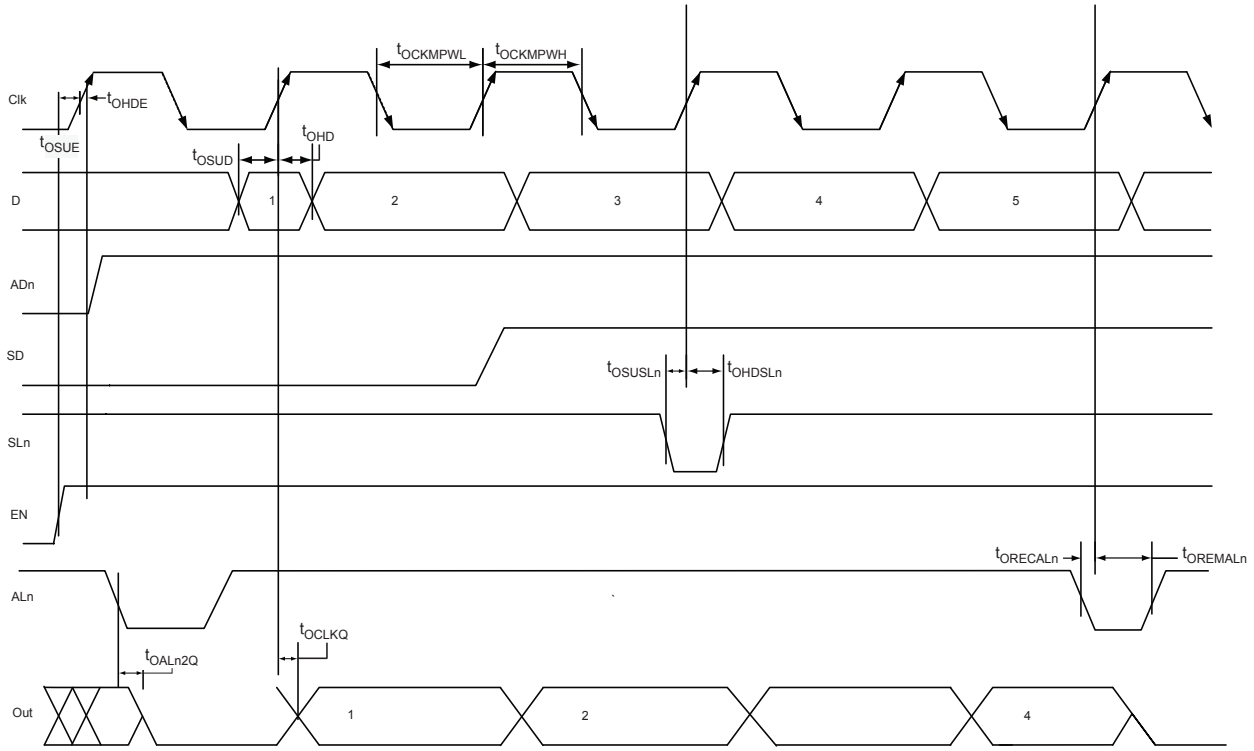


Figure 6 • **I/O Register Output Timing Diagram**

Table 89 • Output Data/Enable Register Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	–1	Std.	Units
t_{OBYP}	Bypass Delay of the Output/Enable Register	F, G or H, I	0.371	0.437	ns
t_{OCLKQ}	Clock-to-Q of the Output/Enable Register	E, G or E, I	0.277	0.326	ns
t_{OSUD}	Data Setup Time for the Output/Enable Register	A, E or J, E	0.2	0.235	ns
t_{OHD}	Data Hold Time for the Output/Enable Register	A, E or J, E	0	0	ns
t_{OSUE}	Enable Setup Time for the Output/Enable Register	B, E	0.441	0.519	ns
t_{OHE}	Enable Hold Time for the Output/Enable Register	B, E	0	0	ns
t_{OSUSL}	Synchronous Load Setup Time for the Output/Enable Register	D, E	0.207	0.243	ns
t_{OHSL}	Synchronous Load Hold Time for the Output/Enable Register	D, E	0	0	ns
t_{OALn2Q}	Asynchronous Clear-to-Q of the Output/Enable Register (ADn = 1)	C, G or C, I	0.531	0.625	ns
	Asynchronous Preset-to-Q of the Output/Enable Register (ADn = 0)	C, G or C, I	0.555	0.653	ns
$t_{OREMALn}$	Asynchronous Load Removal Time for the Output/Enable Register	C, E	0	0	ns
$t_{ORECALn}$	Asynchronous Load Recovery Time for the Output/Enable Register	C, E	0.036	0.042	ns
t_{OWALn}	Asynchronous Load Minimum Pulse Width for the Output/Enable Register	C, C	0.32	0.376	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output/Enable Register	E, E	0.079	0.093	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output/Enable Register	E, E	0.168	0.197	ns

*Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 7 on page 15 for derating values.*

DDR Module Specification

Input DDR Module

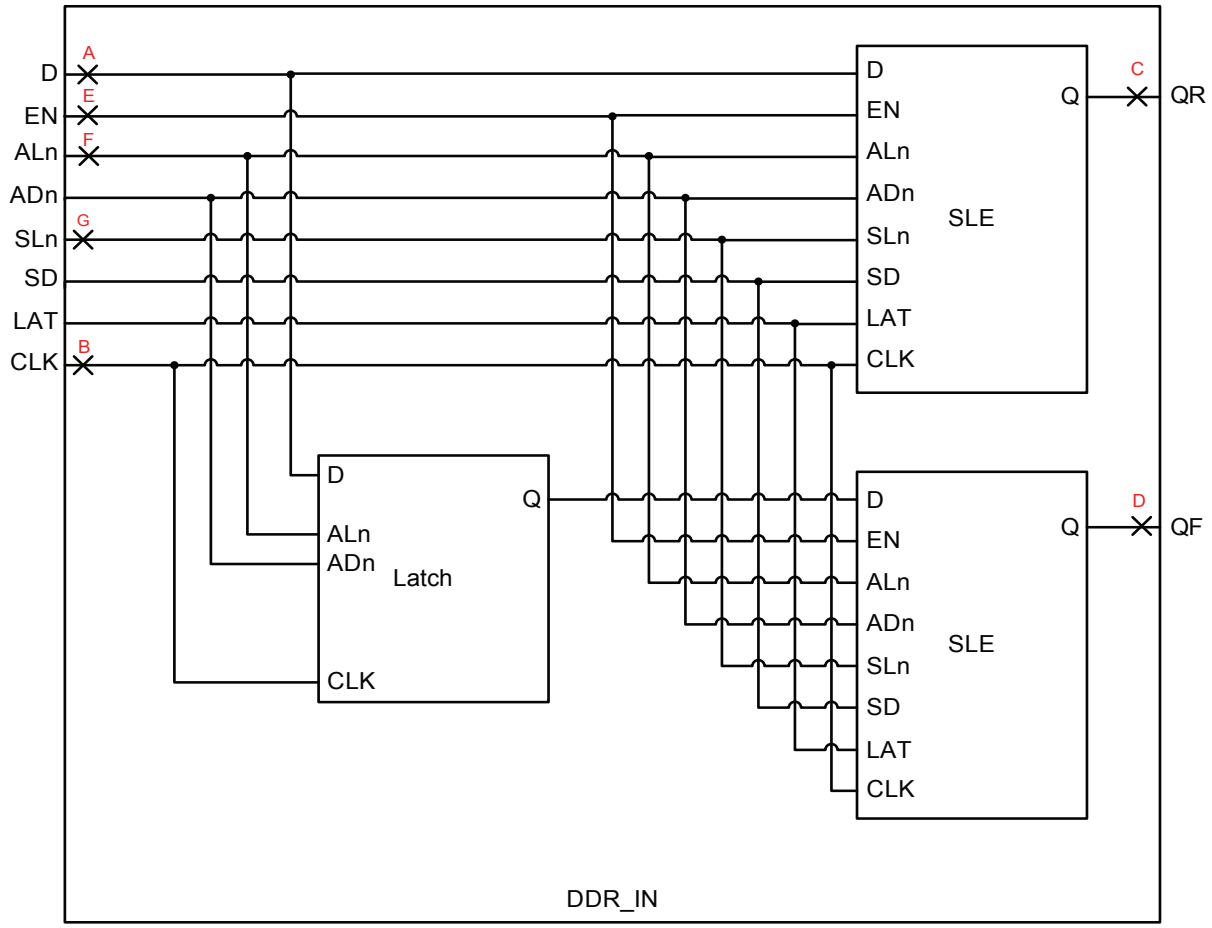


***Figure 7* • Input DDR Module**

Input DDR Timing Diagram

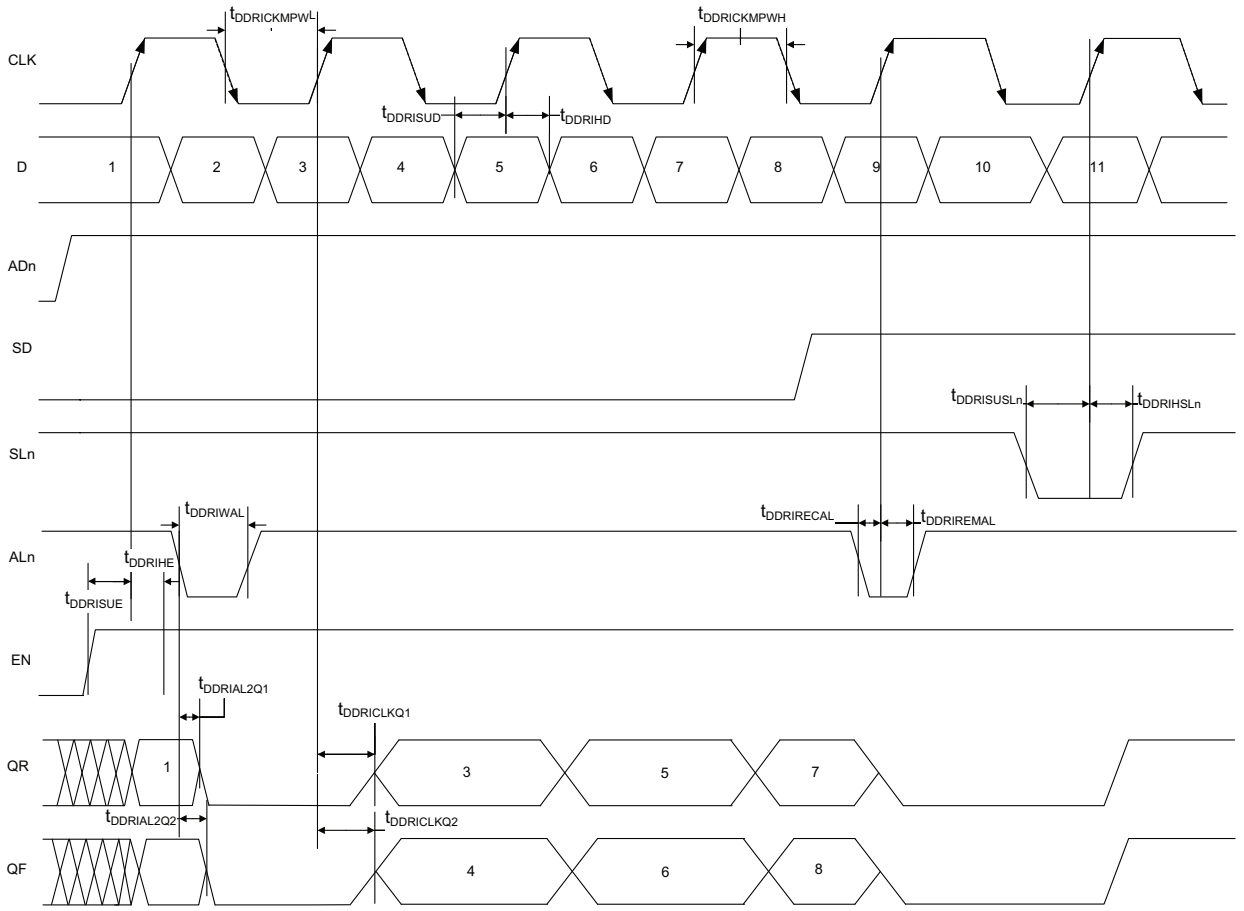


Figure 8 • **Input DDR Timing Diagram**

Timing Characteristics

Table 90 • **Input DDR Propagation Delays**

Parameter	Description	Measuring Nodes (from, to)	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	B, C	0.168	0.198	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	B, D	0.175	0.205	ns
$t_{DDRISUD}$	Data Setup for Input DDR	A, B	0.376	0.443	ns
t_{DDRIHD}	Data Hold for Input DDR	A, B	0	0	ns
$t_{DDRISUE}$	Enable Setup for Input DDR	E, B	0.485	0.57	ns
t_{DDRIHE}	Enable Hold for Input DDR	E, B	0	0	ns
$t_{DDRISUSLn}$	Synchronous Load Setup for Input DDR	G, B	0.485	0.57	ns
$t_{DDRIHSLn}$	Synchronous Load Hold for Input DDR	G, B	0	0	ns
$t_{DDRIAL2Q1}$	Asynchronous Load-to-Out QR for Input DDR	F, C	0.618	0.727	ns
$t_{DDRIAL2Q2}$	Asynchronous Load-to-Out QF for Input DDR	F, D	0.569	0.67	ns
$t_{DDRIREMAL}$	Asynchronous Load Removal time for Input DDR	F, B	0	0	ns
$t_{DDRIRECAL}$	Asynchronous Load Recovery time for Input DDR	F, B	0.078	0.091	ns
$t_{DDRIWAL}$	Asynchronous Load Minimum Pulse Width for Input DDR	F, F	0.32	0.376	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	B, B	0.079	0.093	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	B, B	0.168	0.197	ns

Output DDR Module

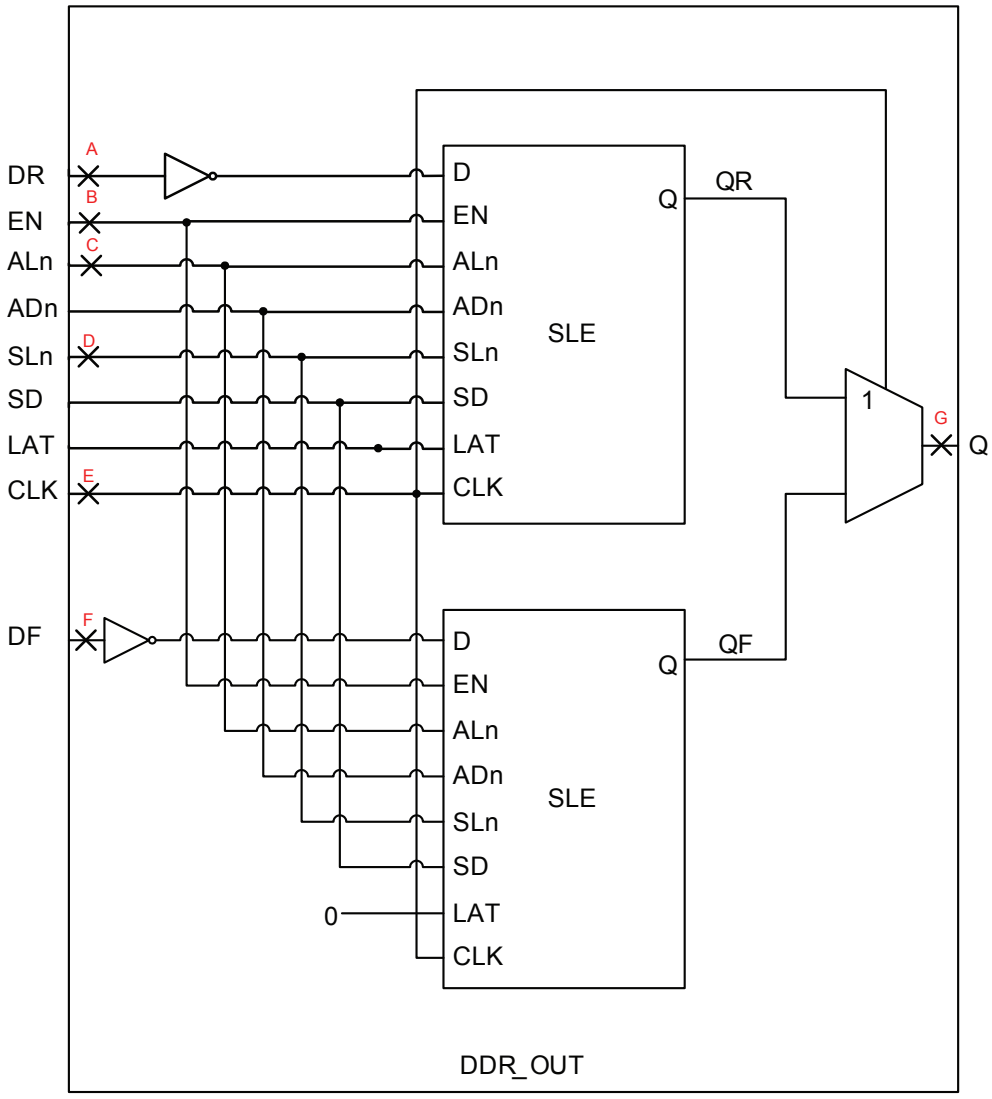


***Figure 9* • Output DDR Module**

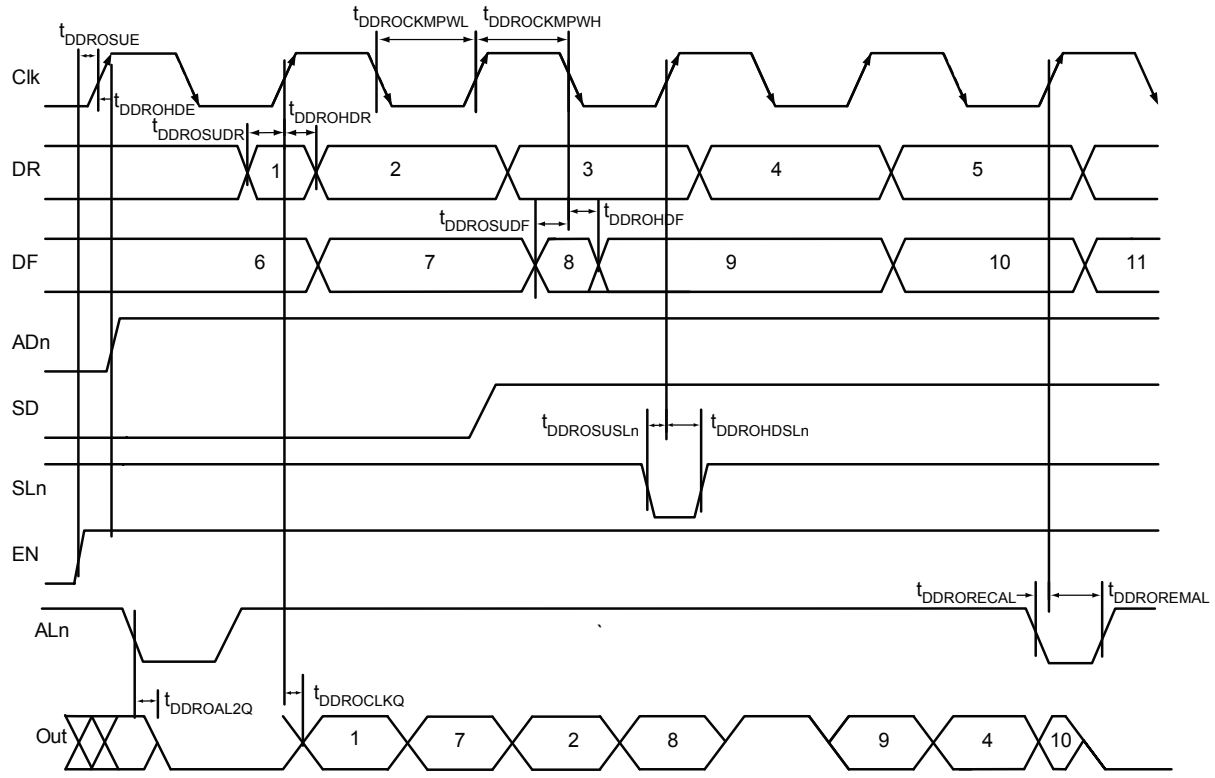


***Figure 10* • Output DDR Timing Diagram**

Timing Characteristics

Table 91 • Output DDR Propagation Delays

Parameter	Description	Measuring Nodes (from, to)	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	E, G	0.277	0.326	ns
$t_{DDROSUDF}$	Data_F Data Setup for Output DDR	F, E	0.151	0.177	ns
$t_{DDROSUDR}$	Data_R Data Setup for Output DDR	A, E	0.2	0.235	ns
$t_{DDROHDF}$	Data_F Data Hold for Output DDR	F, E	0	0	ns
$t_{DDROHDR}$	Data_R Data Hold for Output DDR	A, E	0	0	ns
$t_{DDROSUE}$	Enable Setup for Input DDR	B, E	0.441	0.519	ns
t_{DDROHE}	Enable Hold for Input DDR	B, E	0	0	ns
$t_{DDROSUSLn}$	Synchronous Load Setup for Input DDR	D, E	0.207	0.243	ns
$t_{DDROHSLn}$	Synchronous Load Hold for Input DDR	D, E	0	0	ns
$t_{DDROAL2Q}$	Asynchronous Load-to-Out for Output DDR	C, G	0.555	0.653	ns
$t_{DDROREMAL}$	Asynchronous Load Removal time for Output DDR	C, E	0	0	ns
$t_{DDRORECAL}$	Asynchronous Load Recovery time for Output DDR	C, E	0.036	0.042	ns
$t_{DDROWAL}$	Asynchronous Load Minimum Pulse Width for Output DDR	C, C	0.32	0.376	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	E, E	0.079	0.093	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	E, E	0.168	0.197	ns

Logic Element Specifications

4-input LUT (LUT-4)

The IGLOO2 offers a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO2 Macro Library Guide*.

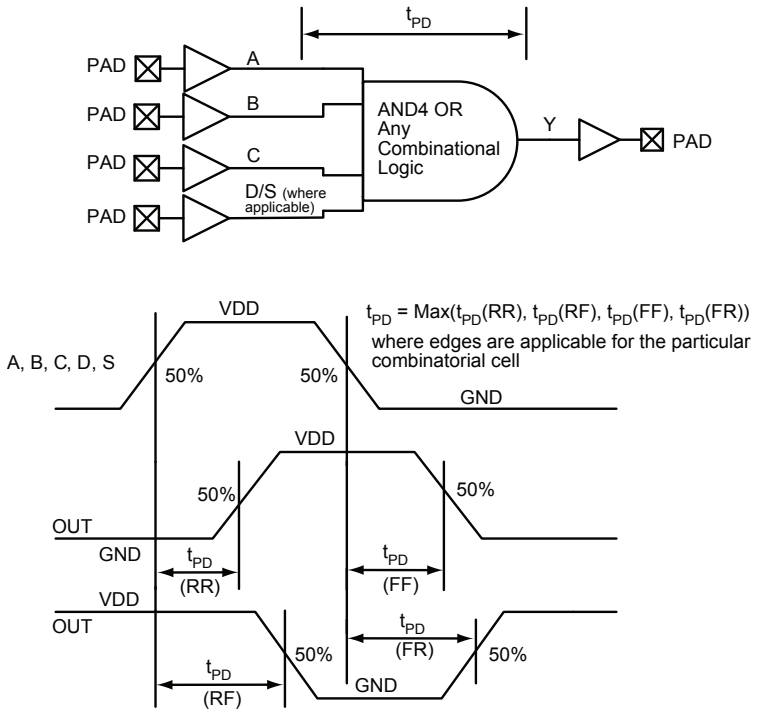


Figure 11 • **LUT-4**

Timing Characteristics

Table 92 • **Combinatorial Cell Propagation Delays**

Combinatorial Cell	Equation	Parameter	–1	Std.	Units	Notes
INV	Y = !A	t_{PD}	0.108	0.127	ns	
AND2	Y = A · B	t_{PD}	0.172	0.203	ns	
NAND2	Y = !(A · B)	t_{PD}	0.16	0.188	ns	
OR2	Y = A + B	t_{PD}	0.172	0.203	ns	
NOR2	Y = !(A + B)	t_{PD}	0.16	0.188	ns	
XOR2	Y = A ⊕ B	t_{PD}	0.172	0.203	ns	
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.253	0.298	ns	
AND3	Y = A · B · C	t_{PD}	0.208	0.245	ns	
AND4	Y = A · B · C · D	t_{PD}	0.383	0.451	ns	

Sequential Module

IGLOO2 offers a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

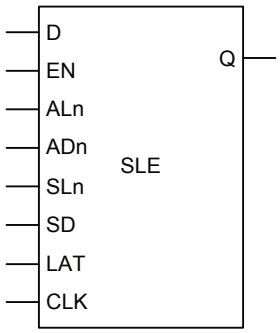


Figure 12 • **Sequential Module**

Figure 13 shows a configuration with SD = 1 (synchronous preset) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

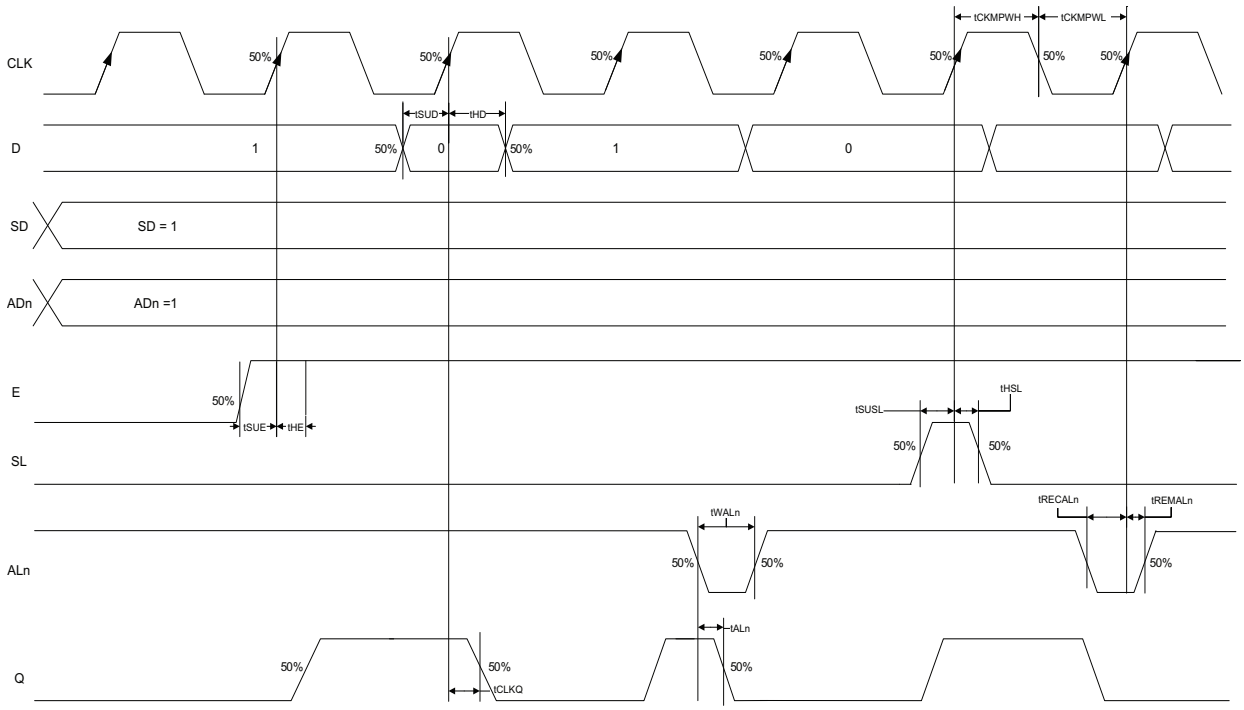


Figure 13 • **Timing Diagram**

Timing Characteristics

Table 93 • **Register Delays**

Parameter	Description	–1	Std.	Units	Notes
t_{CLKQ}	Clock-to-Q of the Core register	0.114	0.134	ns	
t_{SUD}	Data Setup Time for the Core register	0.267	0.314	ns	
t_{HD}	Data Hold Time for the Core register	0	0	ns	
t_{SUE}	Enable Setup Time for the Core register	0.353	0.415	ns	
t_{HE}	Enable Hold Time for the Core register	0	0	ns	
t_{SUSL}	Synchronous Load Setup Time for the Core register	0.353	0.415	ns	
t_{HSL}	Synchronous Load Hold Time for the Core register	0	0	ns	
t_{ALn2Q}	Asynchronous Clear-to-Q of the Core register (ADn = 1)	0.498	0.586	ns	
	Asynchronous Preset-to-Q of the Core register (ADn = 0)	TBD	TBD	ns	
t_{REMALn}	Asynchronous Load Removal Time for the Core register	0	0	ns	
t_{RECALn}	Asynchronous Load Recovery Time for the Core register	0.371	0.437	ns	
t_{WALn}	Asynchronous Load Minimum Pulse Width for the Core register	0.32	0.376	ns	
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core register	0.079	0.093	ns	
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core register	0.168	0.197	ns	

Global Resource Characteristics

IGLOO2 devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the *IGLOO2 FPGA Fabric User's Guide* for the positions of various global routing resources. .

Table 94 • **M2GL150 Global Resource**

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock					ns	
t_{RCKH}	Input High Delay for Global Clock					ns	
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock					ns	
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock					ns	
t_{RCKSW}	Maximum Skew for Global Clock					ns	

Table 95 • **M2GL100 Global Resource**

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock					ns	
t_{RCKH}	Input High Delay for Global Clock					ns	
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock					ns	
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock					ns	
t_{RCKSW}	Maximum Skew for Global Clock					ns	

Table 96 • **M2GL050 Global Resource**

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.804	0.871	0.802	0.872	ns	
t_{RCKH}	Input High Delay for Global Clock	1.494	1.611	1.758	1.895	ns	
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock					ns	
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock					ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.117		0.137	ns	

Table 97 • **M2GL025 Global Resource**

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.725	0.773	0.725	0.774	ns	
t_{RCKH}	Input High Delay for Global Clock	1.362	1.451	1.603	1.705	ns	
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock					ns	
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock					ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.089		0.102	ns	

Table 98 • M2GL010 Global Resource

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.615	0.655	0.614	0.654	ns	
t_{RCKH}	Input High Delay for Global Clock	1.179	1.253	1.386	1.476	ns	
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock					ns	
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock					ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.074		0.09	ns	

Table 99 • M2GL005 Global Resource

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.587	0.619	0.586	0.618	ns	
t_{RCKH}	Input High Delay for Global Clock	1.147	1.211	1.348	1.423	ns	
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock					ns	
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock					ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.064		0.075	ns	

FPGA Fabric SRAM

Refer to the *IGLOO2 FPGA Fabric User's Guide* for more information.

FPGA Fabric Large SRAM (LSRAM)

Table 100 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.352	–	0.414	ns
	Read access time without pipeline register	–	2.392	–	2.815	ns
	Access time with feed-through write timing	–	1.609	–	1.893	ns
t_{ADDRSU}	Address setup time	0.457	–	0.538	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.394	–	0.463	–	ns
t_{DHD}	Data hold time	0.113	–	0.133	–	ns
t_{BLKSU}	Block select setup time (with pipelined register enabled)	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time (with pipelined register enabled)	0.158	–	0.186	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.465	–	0.547	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.586	–	1.865	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.417	–	0.49	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 101 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.352	–	0.414	ns
	Read access time without pipeline register	–	2.392	–	2.814	ns
	Access time with feed-through write timing	–	1.61	–	1.894	ns
t_{ADDRSU}	Address setup time	0.493	–	0.58	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.388	–	0.456	–	ns
t_{DHD}	Data hold time	0.085	–	0.1	–	ns
t_{BLKSU}	Block select setup time	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time	0.158	–	0.186	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.503	–	0.592	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.594	–	1.875	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.443	–	0.522	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 102 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.34	–	0.4	ns
	Read access time without pipeline register	–	2.392	–	2.814	ns
	Access time with feed-through write timing	–	1.591	–	1.872	ns
t_{ADDRSU}	Address setup time	0.564	–	0.664	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.377	–	0.443	–	ns
t_{DHD}	Data hold time	0.085	–	0.1	–	ns
t_{BLKSU}	Block select setup time	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time	0.158	–	0.186	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.536	–	0.631	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.587	–	1.866	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.489	–	0.575	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 103 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.337	–	0.397	ns
	Read access time without pipeline register	–	2.392	–	2.814	ns
	Access time with feed-through write timing	–	1.591	–	1.872	ns
t_{ADDRSU}	Address setup time	0.637	–	0.749		ns
t_{ADDRHD}	Address hold time	0.077	–	0.09		ns
t_{DSU}	Data setup time	0.373	–	0.439		ns
t_{DHD}	Data hold time	0.085	–	0.1		ns
t_{BLKSU}	Block select setup time	0.211	–	0.249		ns
t_{BLKHD}	Block select hold time	0.158	–	0.186		ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.55	–	0.647	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.608		1.892	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.521	–	0.612	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 104 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.337	–	0.397	ns
	Read access time without pipeline register	–	2.388	–	2.809	ns
	Access time with feed-through write timing	–	1.59	–	1.87	ns
t_{ADDRSU}	Address setup time	0.652	–	0.767	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.362	–	0.426	–	ns
t_{DHD}	Data hold time	0.085	–	0.1	–	ns
t_{BLKSU}	Block select setup time	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time	0.158	–	0.186	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.551	–	0.648	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.628	–	1.916	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.485	–	0.57	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 105 • **RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.35	–	0.41	ns
	Read access time without pipeline register	–	2.37	–	2.79	ns
t_{ADDRSU}	Address setup time	0.207	–	0.244	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.389	–	0.458	–	ns
t_{DHD}	Data hold time	0.117	–	0.138	–	ns
t_{BLKSU}	Block select setup time	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time	0.027	–	0.032	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.465	–	0.547	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.05	–	–0.06	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.59	–	1.87	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.29	–	–0.35	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.05	–	–0.06	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.417	–	0.49	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

FPGA Fabric Micro SRAM (uSRAM)

Table 106 • **uSRAM (RAM64x18) in 64x18 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read clock period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.858	–	2.185	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.755	–	2.064	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.055	–	0.064	–	ns
	Read address hold time in asynchronous mode	0.035	–	0.041	–	ns
t_{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t_{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t_{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.173	–	2.556	ns
t_{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.05	–	1.236	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.944	–	1.11	ns
t_{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t_{CCY}	Write clock period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns

Table 106 • **uSRAM (RAM64x18) in 64x18 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{DINCSU}	Write input data setup time	0.017	–	0.02	–	ns
t_{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns
$t_{ADDRCSU}$	Write address setup time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write address hold time	–0.043	–	–0.05	–	ns
t_{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t_{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 107 • **uSRAM (RAM64x16) in 64x16 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read clock period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.858	–	2.185	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.755	–	2.064	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.055	–	0.064	–	ns
	Read address hold time in asynchronous mode	0.035	–	0.041	–	ns
t_{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t_{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t_{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.173	–	2.556	ns
t_{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.044	–	1.228	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.94	–	1.106	ns
t_{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t_{CCY}	Write clock period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t_{DINCSU}	Write input data setup time	0.017	–	0.02	–	ns
t_{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns

Table 107 • **uSRAM (RAM64x16) in 64x16 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
$t_{ADDRCSU}$	Write address setup time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write address hold time	–0.043	–	–0.05	–	ns
t_{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t_{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 108 • **uSRAM (RAM128x9) in 128x9 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read clock period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.898	–	2.233	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.791	–	2.107	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.101	–	0.119	–	ns
	Read address hold time in asynchronous mode	0.082	–	0.096	–	ns
t_{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t_{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t_{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.211	–	2.601	ns
t_{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.042	–	1.226	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.94	–	1.106	ns
t_{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t_{CCY}	Write clock period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t_{DINCSU}	Write input data setup time	–0.025	–	–0.03	–	ns
t_{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns

Table 108 • **uSRAM (RAM128x9) in 128x9 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
$t_{ADDRCSU}$	Write address setup time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write address hold time	0.071	–	0.084	–	ns
t_{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t_{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 109 • **uSRAM (RAM128x8) in 128x8 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read clock period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.898	–	2.233	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.791	–	2.107	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.101	–	0.119	–	ns
	Read address hold time in asynchronous mode	0.082	–	0.096	–	ns
t_{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t_{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t_{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.211	–	2.601	ns
t_{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.042	–	1.226	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.94	–	1.106	ns
t_{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t_{CCY}	Write clock period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t_{DINCSU}	Write input data setup time	–0.025	–	–0.03	–	ns
t_{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns

Table 109 • **uSRAM (RAM128x8) in 128x8 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
$t_{ADDRCSU}$	Write address setup time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write address hold time	0.071	–	0.084	–	ns
t_{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t_{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 110 • **uSRAM (RAM256x4) in 256x4 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read clock period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.933	–	2.275	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.812	–	2.131	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.101	–	0.119	–	ns
	Read address hold time in asynchronous mode	0.082	–	0.096	–	ns
t_{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t_{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t_{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.249	–	2.646	ns
t_{BLKMPW}	Read block select minimum pulse width	–	–	–	–	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	–	–	–	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	–	–	–	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.042	–	1.226	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.94	–	1.106	ns
t_{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t_{CCY}	Write clock period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t_{DINCSU}	Write input data setup time	–0.025	–	–0.03	–	ns
t_{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns

Table 110 • **uSRAM (RAM256x4) in 256x4 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
$t_{ADDRCSU}$	Write address setup time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write address hold time	0.088	–	0.103	–	ns
t_{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t_{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 111 • **uSRAM (RAM512x2) in 512x2 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read clock period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.954	–	2.299	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.849	–	2.175	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.131	–	0.154	–	ns
	Read address hold time in asynchronous mode	0.092	–	0.108	–	ns
t_{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t_{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t_{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.272	–	2.673	ns
t_{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.041	–	1.225	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.937	–	1.102	ns
t_{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t_{CCY}	Write clock period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t_{DINCSU}	Write input data setup time	–0.025	–	–0.03	–	ns
t_{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns

Table 111 • **uSRAM (RAM512x2) in 512x2 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
$t_{ADDRCSU}$	Write address setup time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write address hold time	0.098	–	0.115	–	ns
t_{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t_{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 112 • **uSRAM (RAM1024x1) in 1024x1 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read clock period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.984	–	2.335	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.88	–	2.212	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.131	–	0.154	–	ns
	Read address hold time in asynchronous mode	0.092	–	0.108	–	ns
t_{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t_{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t_{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.299	–	2.705	ns
t_{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.041	–	1.225	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.824	–	0.97	ns
t_{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t_{CCY}	Write clock period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t_{DINCSU}	Write input data setup time	–0.089	–	–0.104	–	ns
t_{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns

Table 112 • **uSRAM (RAM1024x1) in 1024x1 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
$t_{ADDRCSU}$	Write address setup time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write address hold time	0.098	–	0.115	–	ns
t_{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t_{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

On-Chip Oscillators

Table 113 through Table 115 on page 104 describe the electrical characteristics of the available on-chip oscillators in IGLOO2 devices.

Table 113 • **Electrical Characteristics of the Crystal Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
FXTAL	Operating frequency	–	–	32	–	KHz	
ACCXTAL	Accuracy	High Gain Mode (20 MHz)			0.0047	%	
		Medium Gain Mode (2 MHz)			0.00105	%	
		Low Gain Mode (32 KHz)			0.000429	%	
CYCXTAL	Output duty cycle	High Gain Mode (20 MHz)		1	3	%	
		Medium Gain Mode (2 MHz)		1	3	%	
		Low Gain Mode (32 KHz)		1	3	%	
JITPERXTAL	Output Period Jitter (peak-to-peak)	High Gain Mode (20 MHz)		200	300	ps	
		Medium Gain Mode (2 MHz)		1	5	ns	
		Low Gain Mode (32 KHz)		150	300	ns	
JITCYCXTAL	Output Cycle-to-Cycle Jitter (peak-to-peak)	High Gain Mode (20 MHz)		200	300	ps	
		Medium Gain Mode (2 MHz)		1	5	ns	
		Low Gain Mode (32 KHz)		150	300	ns	
IDYNXTAL	Operating current	High Gain Mode (20 MHz)			1.5	mA	
		Medium Gain Mode (2 MHz)			0.3	mA	
		Low Gain Mode (32 KHz)			0.044	mA	
PSRRXTAL	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	
VIHXTAL	Input logic level High		0.9 x VPP			V	
VILXTAL	Input logic level Low				0.1 x VPP	V	
SUXTAL	Startup time (w.r.t. stable oscillator output)	High Gain Mode (20 MHz)			0.8	µs	
		Medium Gain Mode (2 MHz)			4.5	µs	
		Low Gain Mode (32 KHz)			115	µs	

Table 114 • **Electrical Characteristics of the 50 MHz RC Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
F50RC	Operating frequency		–	50	–	MHz	
ACC50RC	Accuracy			1	4	%	
CYC50RC	Output duty cycle			1	3	%	
JIT50RC	Output jitter	Period jitter		200	300	ps	
		Cycle-to-cycle jitter		200	300	ps	
IDYN50RC	Operating current		TBD	6.5	TBD	mA	
PSRR50RC	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	

Table 115 • **Electrical Characteristics of the 1 MHz RC Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
F1RC	Operating frequency		–	1	–	MHz	
ACC1RC	Accuracy			1	3	%	
CYC1RC	Output duty cycle			1	3	%	
JIT1RC	Output jitter	Period jitter		10	20	ns	
		Cycle-to-cycle jitter		10	20	ns	
IDYN1RC	Operating current		TBD	0.1	TBD	mA	
PSRR1RC	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	
SU1RC	Startup time				17	µs	

Clock Conditioning Circuits (CCC)

Table 116 • **IGLOO2 CCC/PLL Specification**

Parameter			Minimum	Typical	Maximum	Units	Notes
Clock conditioning circuitry input frequency f_{IN_CCC}			1		200	MHz	
Clock conditioning circuitry output frequency f_{OUT_CCC}			20		400	MHz	
Delay increments in programmable delay blocks				75	100	ps	
Number of programmable values in each programmable delay block					64		
Acquisition time				70	100	µs	
Tracking jitter				TBD		ns	
Output duty cycle			48		52	%	
Feedback delay					8	ns	
CCC output peak-to-peak period jitter FCCC_OUT	Maximum peak-to-peak period jitter						
	SSO = 0	0 < SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16		
	FG896	FG896	FG896	FG896	FG896		
20 MHz to 100 MHz	110 ps	150 ps				% f_{OUT_CCC}	
100 MHz to 400 MHz	120 ps	150 ps			170 ps	% f_{OUT_CCC}	
Spread Spectrum Characteristics							
Modulation frequency range			25	35	50	kHz	
Modulation depth range			0		1.5	%	
Modulation depth control				0.5		%	

JTAG

Table 117 • **JTAG 1532**

Worst Commercial-Case Conditions: TJ = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units	Notes
t_{DISU}	Test data input setup time			ns	
t_{DIHD}	Test data input hold time			ns	
t_{TMSSU}	Test mode select setup time			ns	
t_{TMDHD}	Test mode select hold time			ns	
t_{TCK2Q}	Clock to Q (data out)			ns	
t_{RSTB2Q}	Reset to Q (data out)			ns	
F_{TCKMAX}	TCK maximum frequency			MHz	
$t_{TRSTREM}$	ResetB removal time			ns	
$t_{TRSTREC}$	ResetB recovery time			ns	
$t_{TRSTMPW}$	ResetB minimum pulse			ns	

*Note: *For specific junction temperature and voltage supply levels, refer to Table 7 on page 15 for derating values.*

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, refer to Figure 14 on page 107.

Table 118 • **SPI Characteristics**
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	M2GL050	M2GL025	M2GL010	Units	Notes
sp1	SPI_0_CLK minimum period					
	SPI_0_CLK = PCLK/2	12			ns	
	SPI_0_CLK = PCLK/4	24.1			ns	
	SPI_0_CLK = PCLK/8	48.2			ns	
	SPI_0_CLK = PCLK/16	0.1			µs	
	SPI_0_CLK = PCLK/32	0.19			µs	
	SPI_0_CLK = PCLK/64	0.39			µs	
	SPI_0_CLK = PCLK/128	0.77			µs	
sp2	SPI_0_CLK minimum pulse width High					
	SPI_0_CLK = PCLK/2	6			ns	
	SPI_0_CLK = PCLK/4	12.05			ns	
	SPI_0_CLK = PCLK/8	24.1			ns	
	SPI_0_CLK = PCLK/16	0.05			µs	
	SPI_0_CLK = PCLK/32	0.095			µs	
	SPI_0_CLK = PCLK/64	0.195			µs	
	SPI_0_CLK = PCLK/128	0.385			µs	
sp3	SPI_0_CLK minimum pulse width Low					
	SPI_0_CLK = PCLK/2	6			ns	
	SPI_0_CLK = PCLK/4	12.05			ns	
	SPI_0_CLK = PCLK/8	24.1			ns	
	SPI_0_CLK = PCLK/16	0.05			µs	
	SPI_0_CLK = PCLK/32	0.095			µs	
	SPI_0_CLK = PCLK/64	0.195			µs	
	SPI_0_CLK = PCLK/128	0.385			µs	
sp4	SPI_0_CLK, SPI_0_DO, SPI_0_SS rise time (10%-90%)	TBD			ns	1
sp5	SPI_0_CLK, SPI_0_DO, SPI_0_SS fall time (10%-90%)	TBD			ns	1
sp6	Data from master (SPI_0_DO) setup time	1	1	1	pclk cycles	2
sp7	Data from master (SPI_0_DO) hold time	1	1	1	pclk cycles	2

Notes:

1. *These values are provided for a load of 5 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *For allowable pclk configurations, refer to the HPMS Configurator User's Guide in Libero to configure the clock in the IGLOO2 High Performance Memory Subsystem User's Guide.*

Table 118 • SPI Characteristics
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade (continued)

Symbol	Description and Condition	M2GL050	M2GL025	M2GL010	Units	Notes
sp8	SPI_0_DI setup time	1	1	1	pclk cycles	2
sp9	SPI_0_DI hold time	1	1	1	pclk cycles	2

Notes:

1. *These values are provided for a load of 5 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *For allowable pclk configurations, refer to the HPMS Configurator User's Guide in Libero to configure the clock in the IGLOO2 High Performance Memory Subsystem User's Guide.*

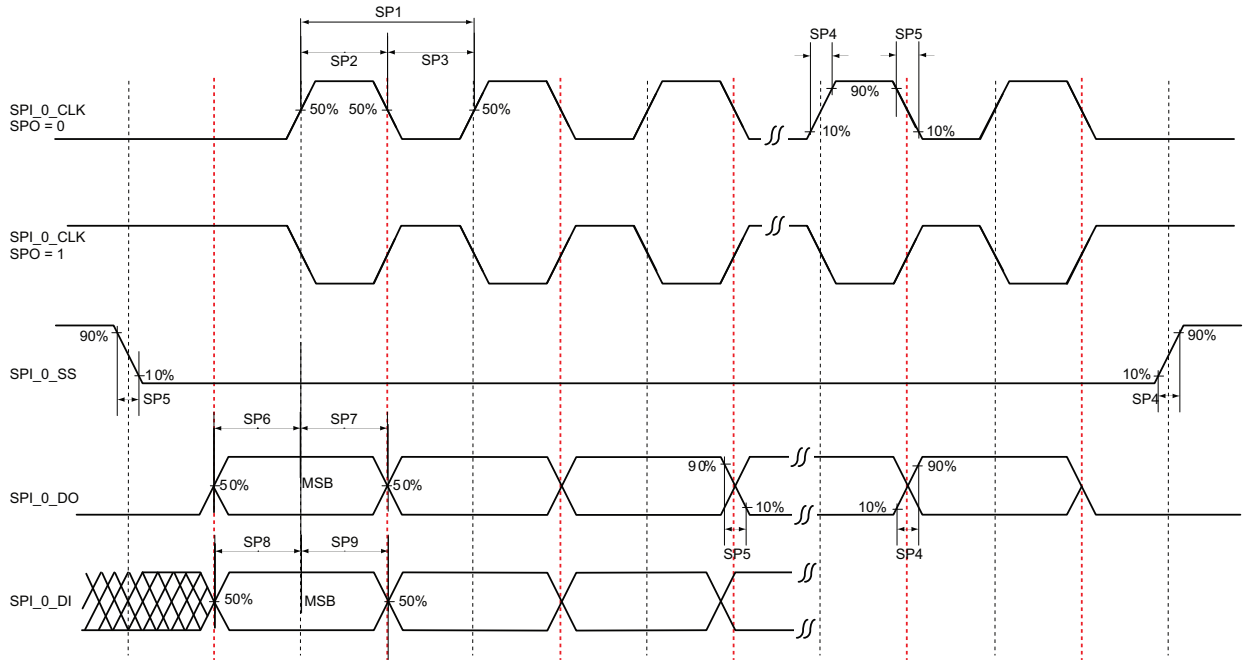


Figure 14 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each SmartFusion mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

Table 119 • **Mathblocks with All Registers Used**

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{MISU}	Input, control register setup time	1.347		1.585		ns	
t_{MIHD}	Input, control register hold time	1.768		2.08		ns	
$t_{MOCDINSU}$	CDIN input setup time	0.195		0.23		ns	
$t_{MOCDINHD}$	CDIN input hold time	0.084		0.099		ns	
$t_{MSRSTENSU}$	Synchronous reset/enable setup time	–0.441		–0.519		ns	
$t_{MSRSTENHD}$	Synchronous reset/enable hold time	0.012		0.014		ns	
$t_{MARSTREM}$	Asynchronous reset removal time	0		0		ns	
$t_{MARSTREC}$	Asynchronous reset recovery time	0.093		0.109		ns	
t_{MOCQ}	Output register clock to out delay		0.244		0.287	ns	
t_{MCLKMP}	CLK minimum period	2.363		2.78		ns	

Table 120 • **Mathblock with Input Bypassed and Output Registers Used**

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{MOSU}	Output register setup time	2.415		2.841		ns	
t_{MOHD}	Output register hold time	1.768		2.08		ns	
$t_{MOCDINSU}$	CDIN input setup time	0.121		0.143		ns	
$t_{MOCDINHD}$	CDIN input hold time	–0.467		–0.549		ns	
$t_{MSRSTENSU}$	Synchronous reset/enable setup time	–0.441		–0.519		ns	
$t_{MSRSTENHD}$	Synchronous reset/enable hold time	0.012		0.014		ns	
$t_{MARSTREM}$	Asynchronous reset removal time	0		0		ns	
$t_{MARSTREC}$	Asynchronous reset recovery time	0.015		0.018		ns	
t_{MOCQ}	Output register clock to out delay		0.244		0.287	ns	
t_{MCLKMP}	CLK minimum period	2.293		2.698		ns	

Table 121 • Mathblock with Input Register Used and Output in Bypass Mode

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{MISU}	Input register setup time	0.157	–	0.185	–	ns	
t_{MIHD}	Input register hold time	0.195	–	0.23	–	ns	
$t_{MSRSTENSU}$	Synchronous reset/enable setup time	0.084	–	0.099	–	ns	
$t_{MSRSTENHD}$	Synchronous reset/enable hold time	–0.013	–	–0.015	–	ns	
$t_{MARSTREM}$	Asynchronous reset removal time	–0.005	–	–0.006	–	ns	
$t_{MARSTREC}$	Asynchronous reset recovery time	0.093	–	0.109	–	ns	
t_{MICQ}	Input register clock to output delay	–	2.652	–	3.12	ns	
$t_{MCDIN2Q}$	CDIN to output delay	–	2.053	–	2.416	ns	

Table 122 • Mathblock with Input and Output in Bypass Mode

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{MIQ}	Input to output delay	–	2.704	–	3.181	ns	
$t_{MCDIN2Q}$	CDIN to output delay	–	2.053	–	2.416	ns	

Table 123 • Flash*Freeze Entry and Exit Times

Symbols	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
TFF_ENTRY	Entry Time	eNVM and HPMS PLL=ON	–	–	150	us	
		eNVM and HPMS PLL=OFF	–	–	200	us	
TFF_EXIT	Exit Time with respect to HPMS PLL Lock	eNVM and HPMS PLL=ON during F*F	–	–	100	us	
		eNVM=ON and HPMS PLL=OFF during F*F and HPMS PLL turned back on at exit	–	–	120	us	
		eNVM and HPMS PLL=OFF during F*F and both are turned back on at exit	–	–	200	us	
		eNVM=OFF and HPMS PLL=ON during F*F and eNVM turned back on at exit	–	–	200	us	
	Exit Time with respect to Fabric PLL Lock	eNVM and HPMS PLL=ON during F*F	–	–	1.5	µs	
		eNVM and HPMS PLL=OFF during F*F and both are turned back on at exit	–	–	1.5	µs	
	Exit Time with respect to Fabric buffer output	eNVM and HPMS PLL=ON during F*F	–	–	15	us	
		eNVM and HPMS PLL=OFF during F*F and both are turned back on at exit	–	–	55	us	

PCIe Electrical and Timing AC and DC Characteristics

PCIe is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 family has two hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 124 • **Transmitter Parameters**

Parameter	Description	Min.	Typ.	Max.	Units	Notes
VTX-DIFF-PP	Differential swing PCIe Gen 1 and 2	0.8	–	1.2	mV	
VTX-CM-AC-P	Output common mode voltage PCIe Gen 1	–	–	20	mV	
VTX-CM-AC-PP	Output common mode voltage PCIe Gen 2	–	–	100	mV	
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen 1	0.125	–	–	UI	
	Rise and fall time (20% to 80%) PCIe Gen 2	0.15	–	–	UI	
ZTX-DIFF-DC	Output impedance – differential	80	–	120	ohm	
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen 1	–	–	500 ps + 2 UI	ps	
	Lane-to-lane TX skew within a SERDES block PCIe Gen 2	–	–	500 ps +4 UI	ps	
RLTX-DIFF	Return loss differential mode PCIe Gen 1	–10	–	–	dB	
	Return loss differential mode PCIe Gen 2	–10 (min.) 0.05 – 1.25 GHz – 8 (min.) 1.25 – 2.5 GHz			dB	
RLTX-CM	Return loss common mode PCIe Gen 1 and 2	–6	–	–	dB	
	Transmit PLL lock time from reset	–	–	10	µs	

Table 125 • **Receiver Parameters**

Parameter	Description	Min	Typ	Max	Units	Notes
VRX-DIFF-PP-CC	Input levels PCIe Gen 1	0.175	–	1.2	mV	
	Input levels PCIe Gen 2	0.12	–	1.2	mV	
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	-	
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV	
VRX-DIFF-PP-CC	Differential input sensitivity PCIe Gen 1	0.175	–	–	mV	
	Differential input sensitivity PCIe Gen 2	0.12	–	–	mV	
ZRX-DIFF-DC	Differential input termination	80	100	120	Ohms	
REXT	External calibration resistor	1,188	1,200	1,212	Ohms	
	CDR relock time from reset	–	–	15	µs	
RLRX-DIFF	Return loss differential mode PCIe Gen 1	–10	–	–	dB	
	Return loss differential mode PCIe Gen 2	–10 (min.) 0.05 – 1.25 GHz –8 (min.) 1.25 – 2.5 GHz			dB	
RLRX-CM	Return loss common mode PCIe Gen 1 and 2	–6	–	–	dB	
	CID limit (set by 8B/10B coding, not the receiver PLL)	–	–	4	UI	
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65	–	175	mV	

Table 126 • SERDES Reference Clock AC Specifications

Symbols	Description	Conditions	Min.	Typ.	Max.	Units	Notes
FREFCLK	Reference Clock Frequency		100		160	MHz	
TRISE	Reference Clock Rise Time		0.6		4	V/ns	
TFALL	Reference Clock Fall Time		0.6		4	V/ns	
TCYC	Reference Clock Duty Cycle		40		60	%	
Mmrefclk	Reference Clock Mismatch		-300		300	ppm	
SSCref	Reference Spread Spectrum Clock		0		5000	ppm	

Datasheet Information

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO2 Device Status" table on page 1 is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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